WERSI

assembly manual

Technical Data
CD 600/700/800/900

AM 320 1st Edition

TABLE OF CONTENTS

I. PURPOSE OF THIS MANUAL

This manual is supposed to complement the assembly manuals and the User's Guides by presenting the technical principles behind the operation of the CD 6/7/8/900 organs. It is not necessary to know the information given in this manual to assemble the organ. However. it is possible to gain a better understanding of the musical possibilities of the organ by learning the technical aspects of its operation. Also, knowing such information can be a big help if you ever - hopefully never - have to troubleshoot the organ.

The technical data is presented in a manner that is aimed more at the interested layman than the electronic specialist. Rather than going into fine detail about how each circuit functions, the text gives more of an overview of how the various subassemblies and modules work.

11. TECHNICAL CONCEPT

A. Traditional Organ Systems

To put the new CD digital organ concept in proper perspective, we will first briefly look at three approaches to electronic organ technology.

1. AnalogOrgans

In this type-and this is the type most commonly used-sine wave. tones are produced by a tone generator, selected by mechanical or electronic switches, processed in filters to produce the desired voicing, amplified and applied to a speaker.

Of interest here is that it is the hardware (the system components) alone that determines the capabilities of such an instrument.

2. Quasi-Digital Organs

These organs are touted as being "digital;' especially in the promotional literature, but a closer look shows that they do not merit this tag. To be sure, they employ digital support techniques-serial data transmission, for example-along with complex IC circuitry. But the tones are still developed and processed mainly by analog means.

3. Digital Systems Using Original Sounds in Memory

Committing original musical sounds to a digital memory is a widely know technique used in digital synthesizers and rhythm units. In moderately priced instruments, reflecting moderate technical sophistication, the sounds of instruments such as trumpets, violins and pianos are stored exactly as those of drums, cymbals or cowbells-in short, single tones.

These original tones are read out when the instrument is played and are assigned to the desired instrument range according to a clock frequency controlled from the keyboard. A digital-to-analog converter changes the digital data back into audible analog tones. The tones sound rather genuine when played in the tonal range of the original instrument; however, the tones become less and less true the further the player deviates from this range. This is because the tone formants cannot be held constant over the entire range of the keyboard.

B. The CD System With Full Digital Tone Processing

In this new Wersi technology, a microprocessor system computes all the sounds and digital.to-analog conversion produces audio tones from the resulting data. The processor system consists of a master processor and up to eight co-processors, known as slaves.

The slaves are responsible for the correct processing of the tones, receiving essential data such as pitch, volume (envelope amplitude), frequency, vibrato, formants, etc. from the master processor. The master processor sends new data to the slave anytime there is a change in input status, whether it is a registration change or a new key stroke.
The outstanding advantage of this system is that a wide range of musical forms can be achieved, even though the hardware never changes. It is the software-data programs read into the organ from a memory card or a computer-that creates so many musical possibilities. The data in the organ's memories can be added to or changed completely, giving the organ a whole new repertoire, if desired. Sounds from liturgical organ to synthesizers to conventional musical instruments are possible through software.

A further advantage of this system is that a given sound quality, once achieved and filed as software, will be the same when reproduced by any organ in the series, since hardware variations will have virtually no effect on the sound properties.

Additional special effects can be achieved through further processing of the digitally developed voices via a voltage-controlled filter (VCF) and a phase vibrato (Wersivoice) circuit.

Apart from its contrast to other organ systems, the CD concept offers the most possibilities in terms of sound and functions, and is the most flexible concept for the electronic production of individual musical voices yet presented.

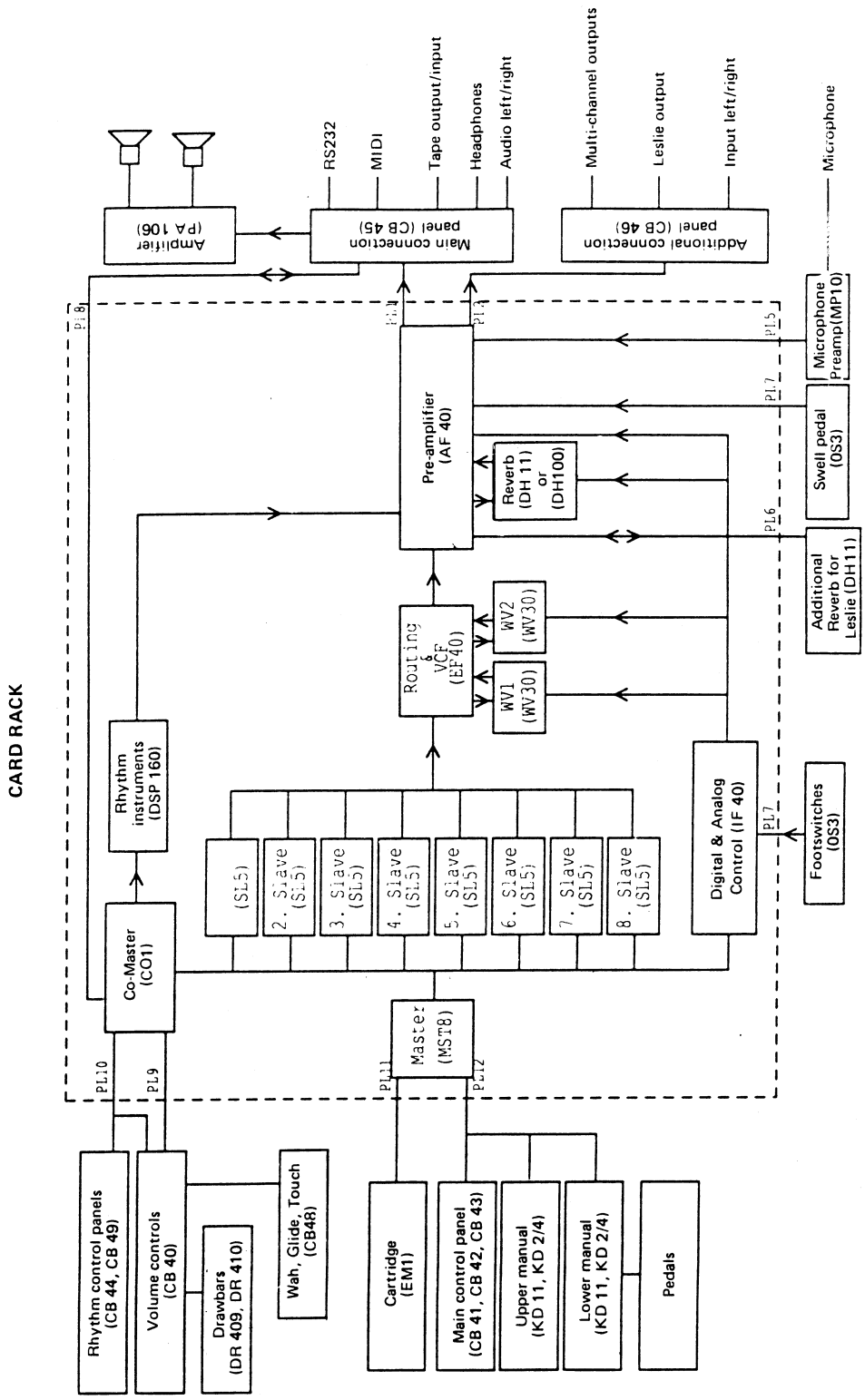
C. The CD System Block Diagrams

1. The Complete Organ

The master (MST8) contains the Central Processing

Unit **(CPU) of the organ. When a key is played on the key**boards or pedalboard, the CPU gathers all of the information required to produce that tone from its memory **and sends this information to one of the slave (SL5)**
units. It is here that the tone is actually produced. The tone, after leaving the slave, may receive additional analog effects (Wersivoice, VCF, etc.) as desired.

The master (MST8) is supported in its work by the co-master (COl), which monitors the volume controls and drawbars, as well as controlling the rhythm unit and managing the MIDI and RS-232 interfaces.



Block Diagram CD Series

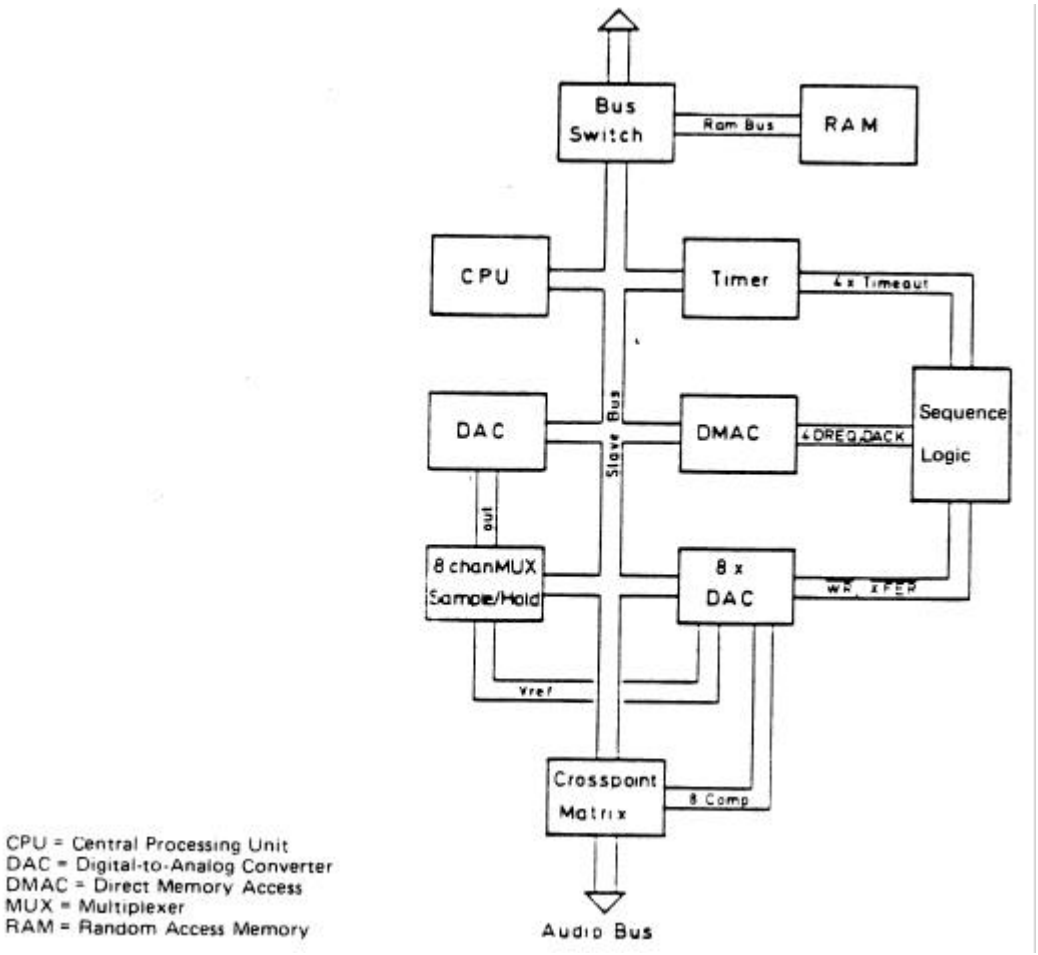
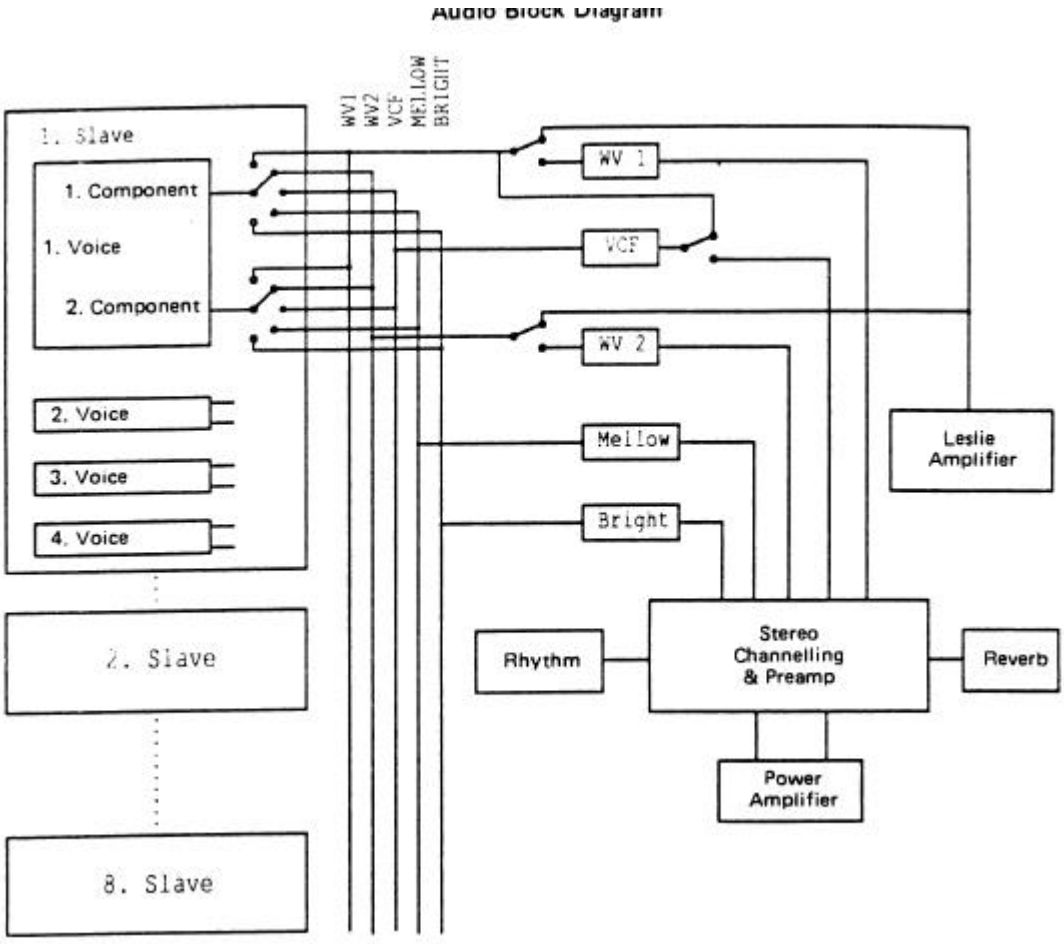


Fig. 2: Block diagram of a slave processor

2. The Slave Processor (5L5)

The slaves can be thought of as digital sound generators. Each SL5 board can produce 4 sounds, each consisting of two sound components; the organ can be equipped with a total of 8 slave boards.

The slave receives its information from the master via the 2-port RAM, located on the slave. According to the information it receives from the master, the slave then produces the sounds. The output of the sounds is done automatically by the timer, the DMA controller and the slave CPU after the CPU has made the correct timer and DMA settings. The CPU is responsible only for the amplitude envelope for the 8 components. Each of the B Digital to Analog Converters (DAC) receives an envelope voltage. The Audio signal, after being produced by the DAC, can then be routed to one of the 5 output channels by the "crosspoint matrix."



3. Audio Block Diagram

The audio signals from the slaves are routed to one of five audio channels where they are refined and processed differently:

a)the Bright slave signal reaches the amplifier without any modification.
b) the Mellow slave signal is routed to the amplifier via a low-pass filter.
c)the WV1 slave signal is assigned to Wersivoice 1.
d) the WV2 slave signal is assigned to Wersivoice 2.
e)VCF - further processing of the signal for VCF effects.

The effect channels WV1, WV2 and VCF can be individually assigned to the left or right audio channel; the mellow/bright channels, however, are permanently routed to Left or Right.

4. Digital Rhythm Instruments

Although the functional sequencing of the rhythm unit is completely controlled by the co-master (CO1), the actual sound generation takes place on the instrument board (DSP16O), which carries the digitally stored instruments. For internal control and processing purposes, this module has its own microprocessor. Its audio output is applied directly to the preamp.

5. Digital Reverb Unit

The digital reverb unit is a processor-supported "Real Time System"; its CPU controls the A/() conversion, the digital delay and the D/A conversion. The master controls the reverb modes. It receives its signal from and sends the reverberated signal to the preamp.

6. Connection Panels

The main connection panel CB45 is equipped with three audio outputs:

-Headphones
-Audio left, Audio right
-Tape.

With the additional connection panel CB46 you have a few additional in- and outputs at your disposal:

-Input left/right
- Organ output left/right
- Rhythm unit output left/right
- Reverb output left/right
- Mono/Bass (organ and rhythm unit outputs combined)
- Leslie output with control signals SLOW and FAST

.

Ill. SCHEMATIC DIAGRAMS

In this chapter you will find detailed schematic diagrams, principles of operation and useful tips for everyday practice. In order to give you a better overview, we divided the schematic diagrams into 3 groups as follows:

A Central Electronics
B. Control Panels
C. Peripheral Boards

A. Central Electronics

In this section you will find the pin assignment and the circuitry of the backplane board MB4O and the schematic diagrams of all plug-in boards.

1.MB4O (Backplane PC Board)

This PC board has three basic functions:

- it is the mechanical support for all plug-in boards,
- it connects the boards electrically,
- it carries all connectors for connecting the peripheral modules via ribbon cables.

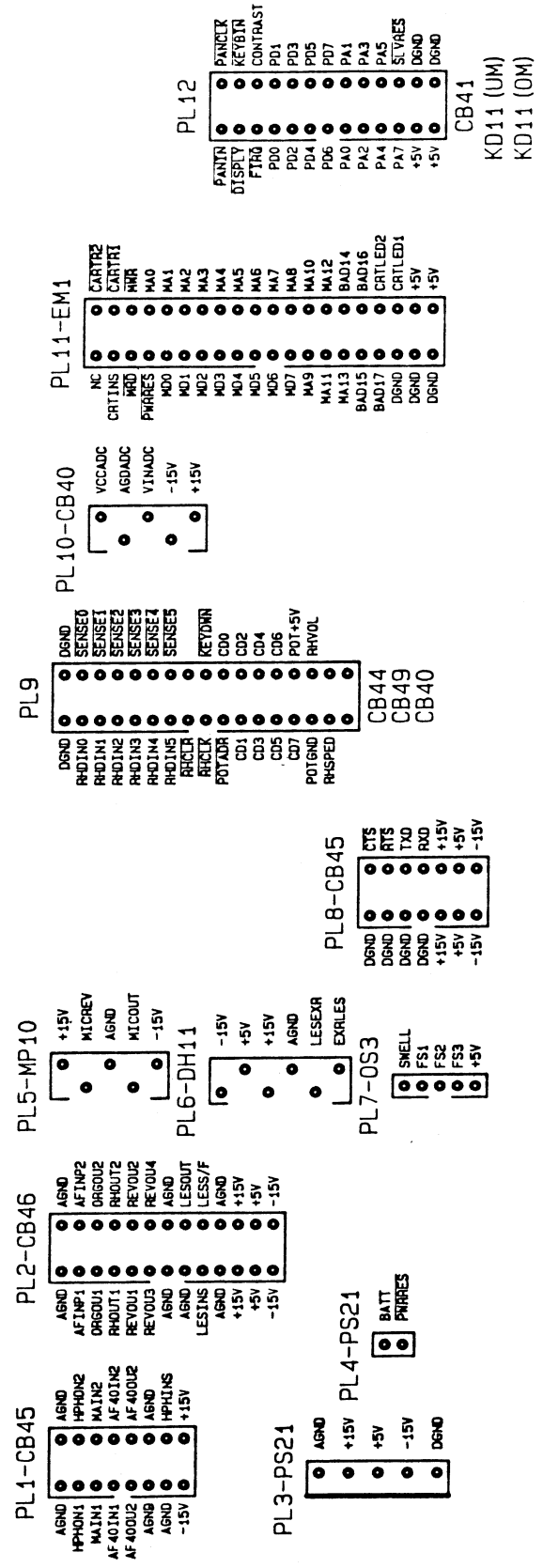
The following figures show the edge connector pin layouts, the male connector pin layouts and the circuitry on the MB 40.

Tip:

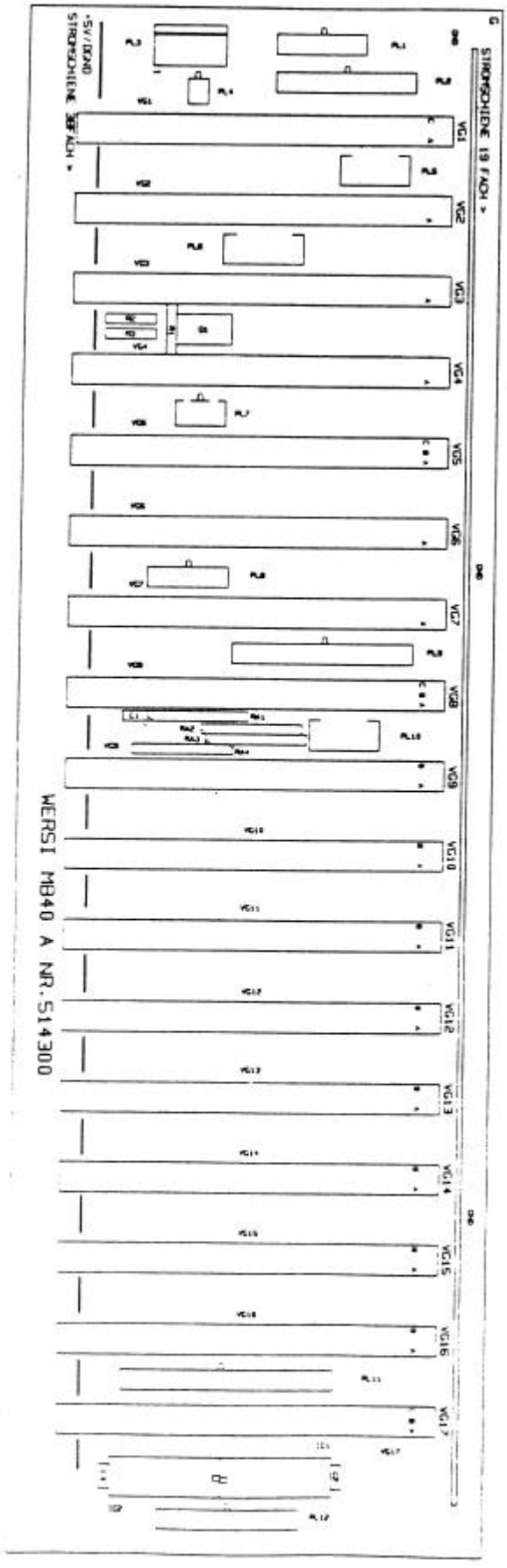
For testing or troubleshooting a plug-in board, pull out the desired card from the card rack, insert the extender card EXT 1 0 (= testing adapter) into the slot of the plug-in board and plug the board to be tested into the EXT 10. Via the solder pins on the EXT 10 all connections are led to the outside and now you may test the accessible components.

Except for the eight slave boards (5L5) and the two WERSIVOICE plug-in boards (WV30), which can be interchanged in their designated slots, no plug-in board must ever be plugged into any slot other than that designated for it.

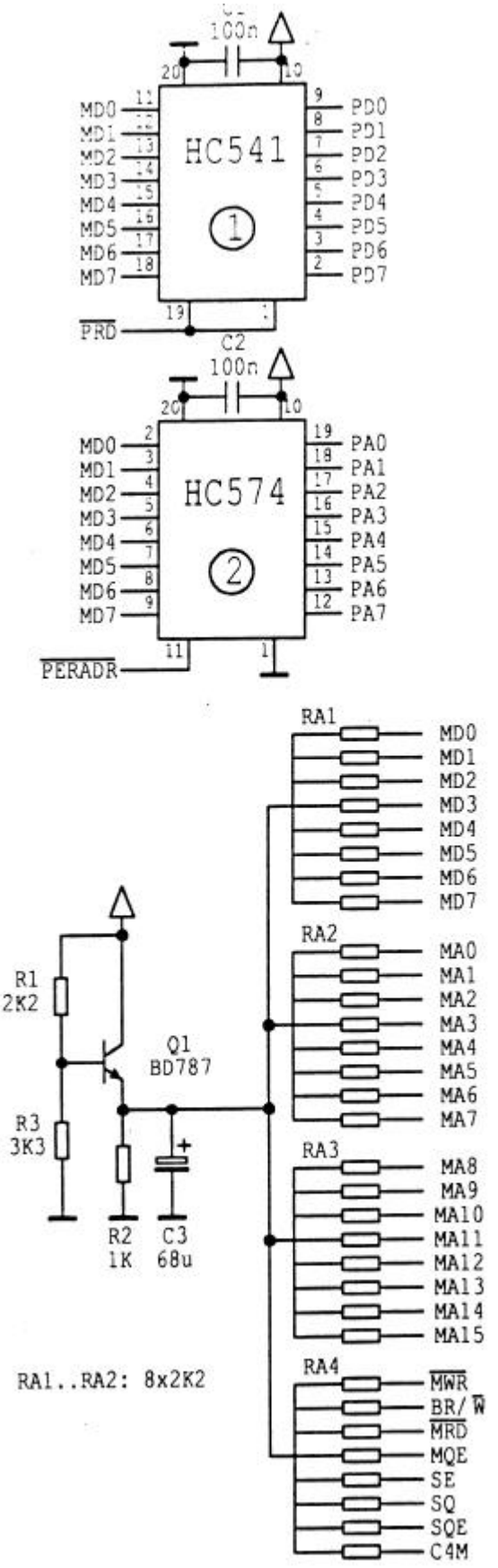
Backplane board MB4O, edge connector pin layout (view from back of card rack



MB4O, Male connector pin layout



MB4O Component layout



MB4O Schematic diagram

2. MST8 (Master)

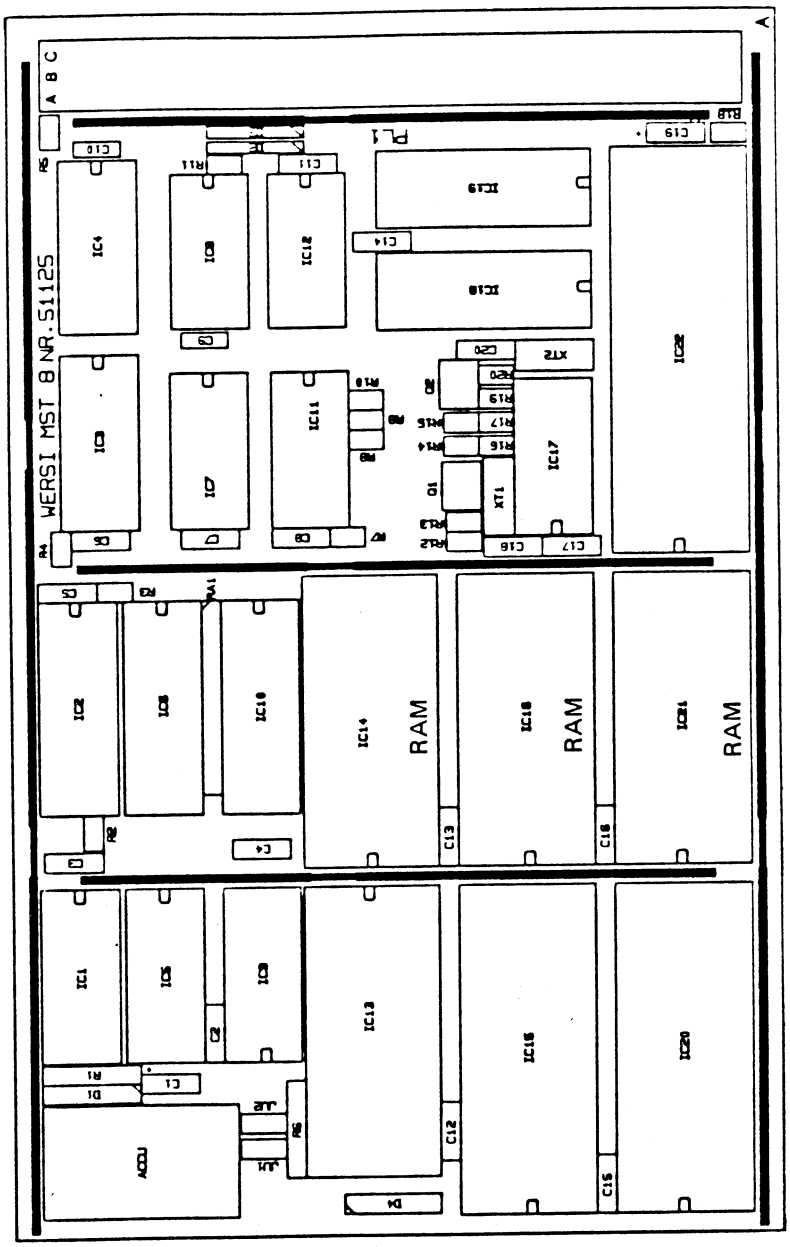
The heart of this board is the CPU 68809. Its address connections are buffered by IC 18 and IC 19 (HCT541) and are increased to a CMOS level. IC 10 (HC245) serves the same function for the data bus. However, this driver is active only if the memory is addressed externally (EXTERN). It remains inactive if RAM, ROM or timers are addressed. IC 15 (SYSROM) contains the System Program, while the Basic Instruments and Presets are stored in IC 20 (IROM). RAM IC 14 (6264) is the CPU's working storage. IC 16 and IC 21(62256) provide 64 k freely programmable instrument and preset storage. The three RAMs are battery-buffered to prevent loss of the memory contents when switching off the power supply. When the supply voltage is stopped, Q1 and Q2 prevent undefined voltage levels from reaching the CS input; this would cause the complete loss of the memory contents. As displayed in the Memory Map, IC 2 (PAL 16L8) IC 9 (HC138) and IC 3 (HC139) are responsible for the distribution of the memory areas into RAM, ROM, I/O, etc. The banking in the lower 16 k of the CPU address region is controlled by the bank latch IC 6 (HC273) the higher outputs of which (BS4-B56) are decoded by IC 1
.

To integrate parts of the SYSROM (IC 15) into this address region, the higher addresses of the SYSROM SA14-SA17 are produced by IC 5 (HC137). Depending on the PROGRAM signal either the addresses MA 14 and MA 15 are switched through or the bank addresses BAD14-BAD1 7.

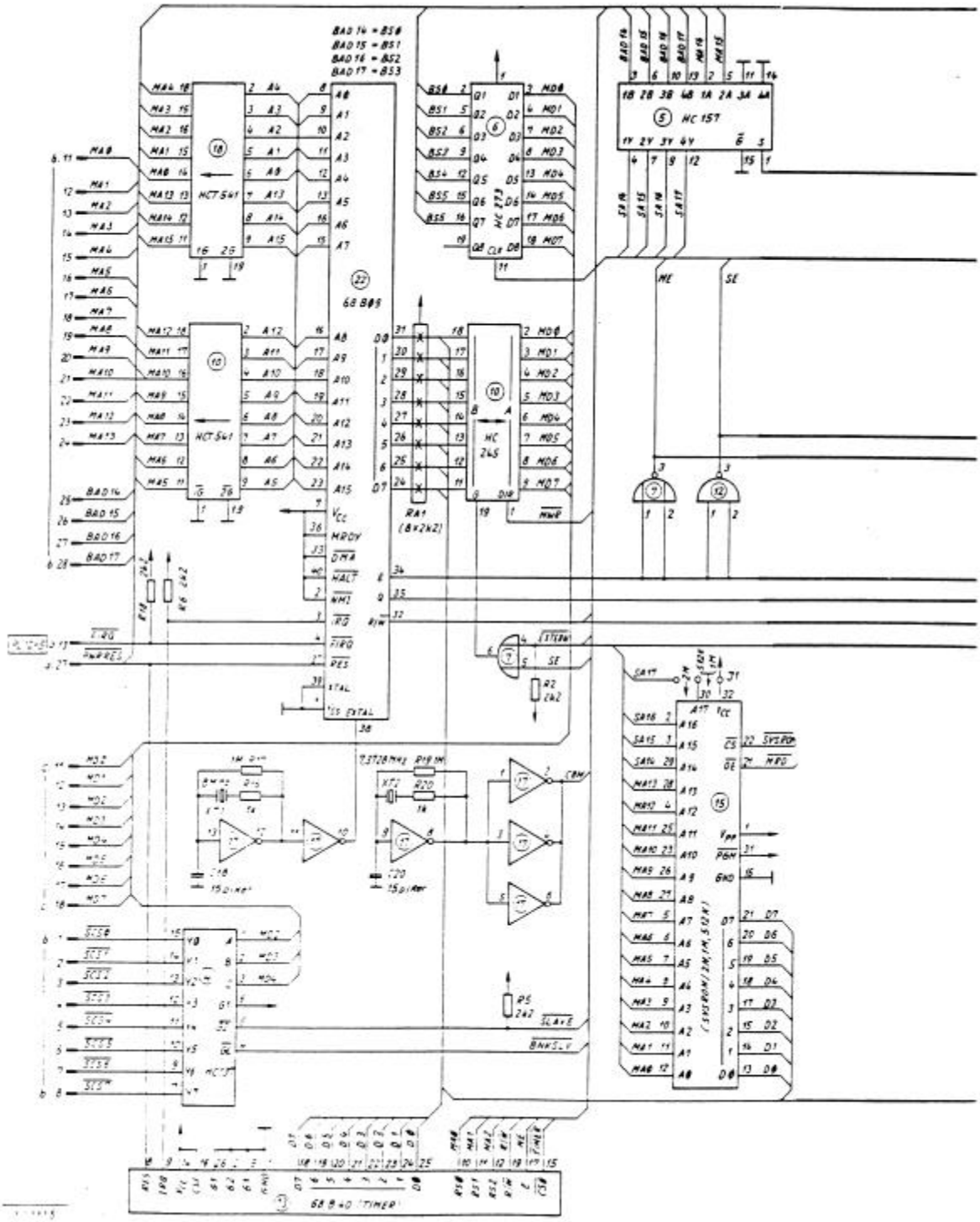
IC 4 (HC137) produces the slave CS signals. The slave number is written into the latch of the HC137 via MD2-MD4 with BNKSLV; if addressed, the number appears decoded in the slave RAM region ($6000. .$67ff) at the outputs SCSO. .$CS7.

The gates IC 7 (HC32), IC 11 (HCOO), IC 8 and IC 12 (ACOO) produce all control signals required by the system.

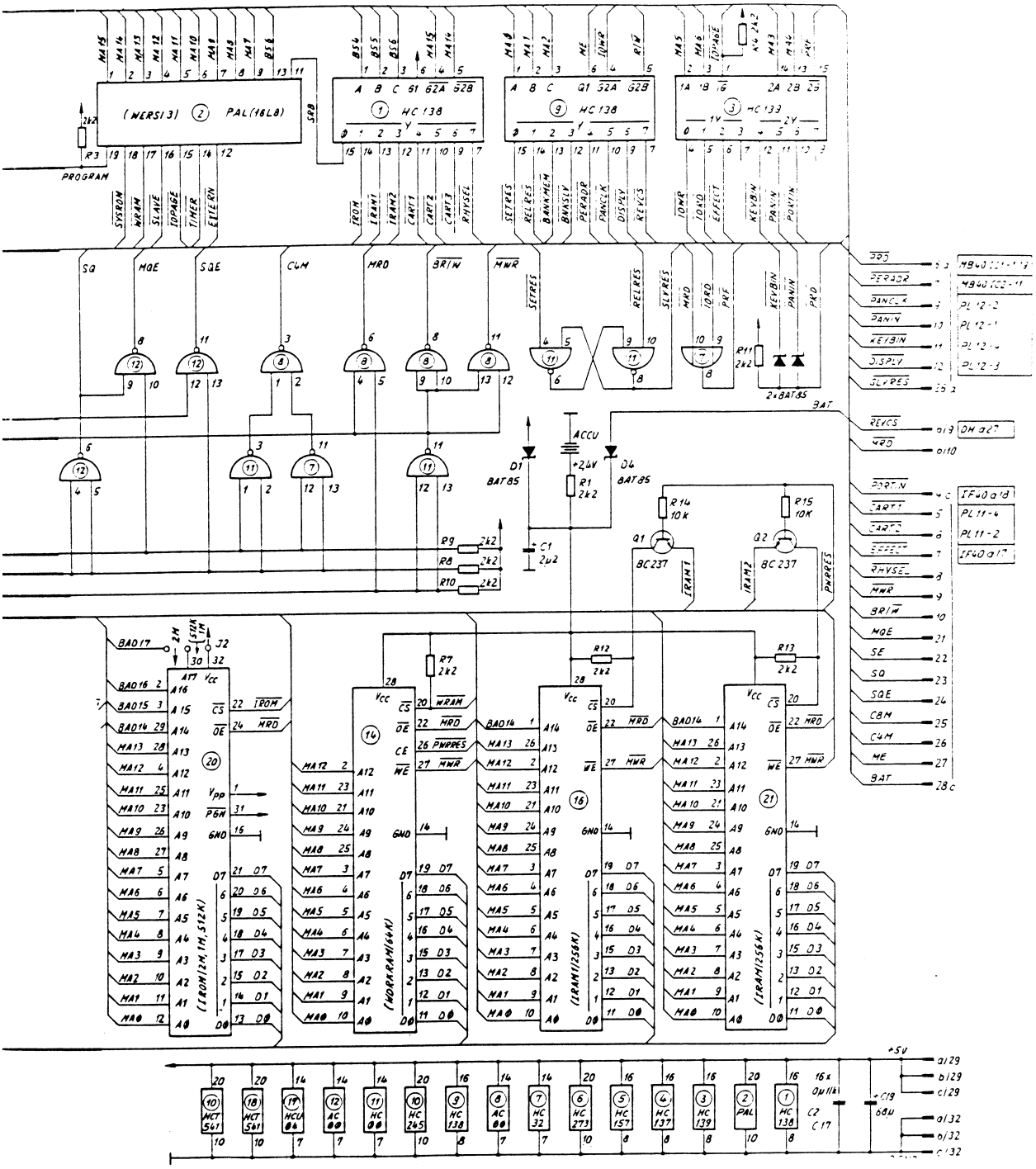
The clock for the timers on the slaves (C8M) is produced on the MST8 as well.



MST8, Component layout



MST8, Schematic diagram



3. SL 5 (Slave)

Each slave produces up to four freely programmable, complex sounds with two sound components each. The sounds can be assigned to the upper manual, lower manual, accompaniment unit, MIDI or pedalboard as desired. Also, several voices can be combined for one instrument.

Since each sound consists of two Waves, eight "audio channels" are necessary for the four voices (IC 10-IC 17 = DAC0832, IC 1-IC 4 = TL084).

As soon as a manual or pedalboard key is depressed, the master loads the "2-Port-RAM" (IC 9, 6264) with the sound parameters via the master bus. For internal processing purposes, the "bus switch" switches the RAM over to the slave bus: with IC 25, 26, 32, 33 (HC 157) the addresses and control signals coming from slave and master are fed through to the RAM, depending on the bus that is given access to the RAM. Via the data bus driver IC 21 (HC1245 for slave bus) and IC 22 (HC245 for master bus), master and slave can read the RAM or write on it.

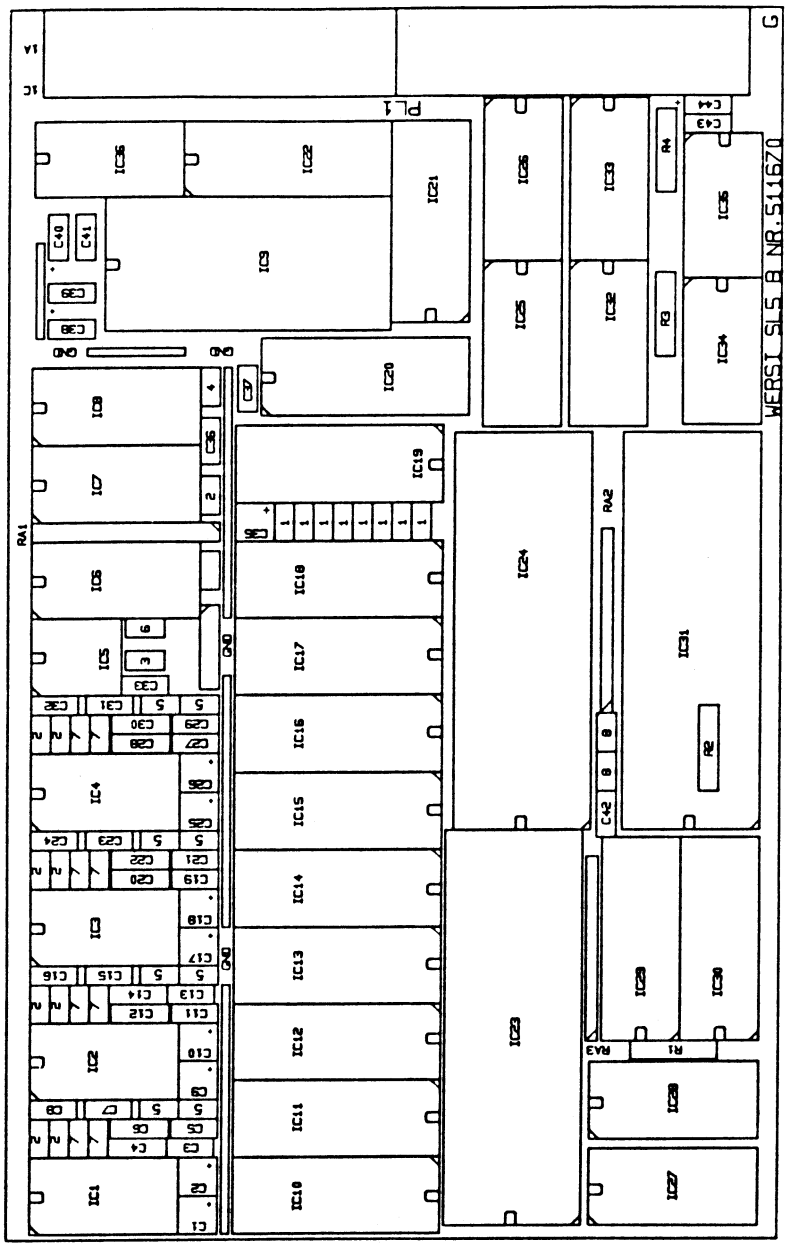
To guarantee optima! data transfer, the cycle times 2MHz) between master and slave processor (ME, MO to master, SE, SO tor slave) are shifted by one half cycle. Thus, also large data packages, for instance for complex voices, can be read in and out with a quasi 4MHz cycle time because the bus switch is constantly switching over from master to slave bus and vice versa, so that both processors have permanent access to the
RAM.

After loading the RAM (by the master), the slave CPU starts and works off the internal program. By programming the timer (IC 23, 9513), the readout rate is determined. Four timers determine the pitch (read-out rate of the sound parameter lists) and the fifth timer determines the' repeat frequency for computing the envelope curve.

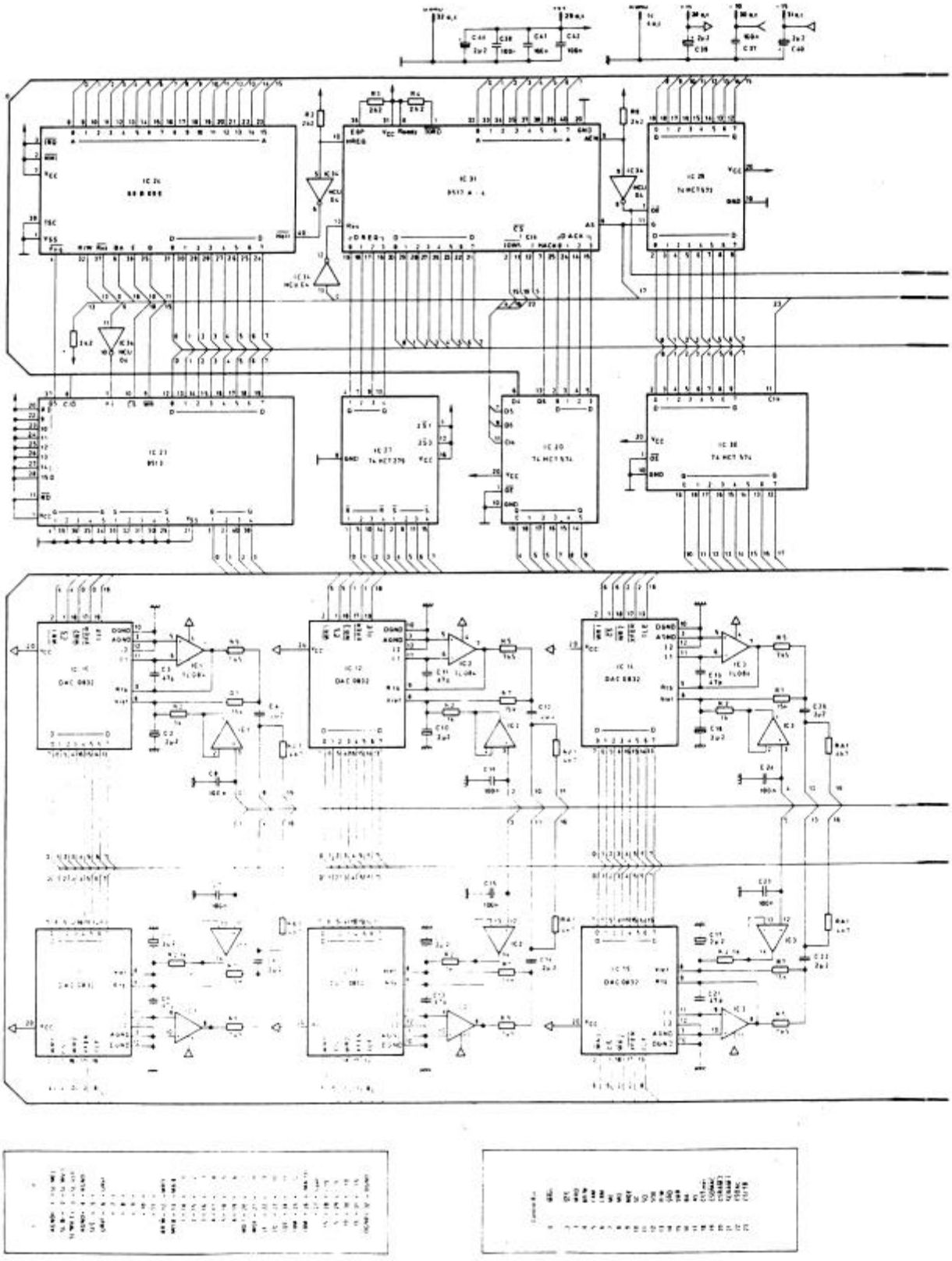
Via the sequence logic (IC 27 = HCT279, IC 20 = HCT-574), the DMA controller (IC 31, 9517) and the eight Wave DACs are controlled, which guarantees output of the sound lists from the RAM without influence by the CPU. The digital values for four voices with two components each are loaded into the eight signal DACs (Write) and converted into analog signal, if permission is given (data transfer = XFER). Due to the fact that the interim storage and the read-out process of the digital information are controlled directly by the timer, correct and undistorted analog signals are produced, independent of internal work cycles.

At the same time, the envelope DAC (IC 18, DAC1232) converts its digital information for eight voice components. Via the 8-channel de-multiplexer (IC 6, 4051) and the Sample&HoId stages (IC 1-IC 4a, d, TL084), the eight envelope voltages are distributed among the eight signal DACs, which act as multiplying DACs and directly determine the volume levels of the respective analog signals.

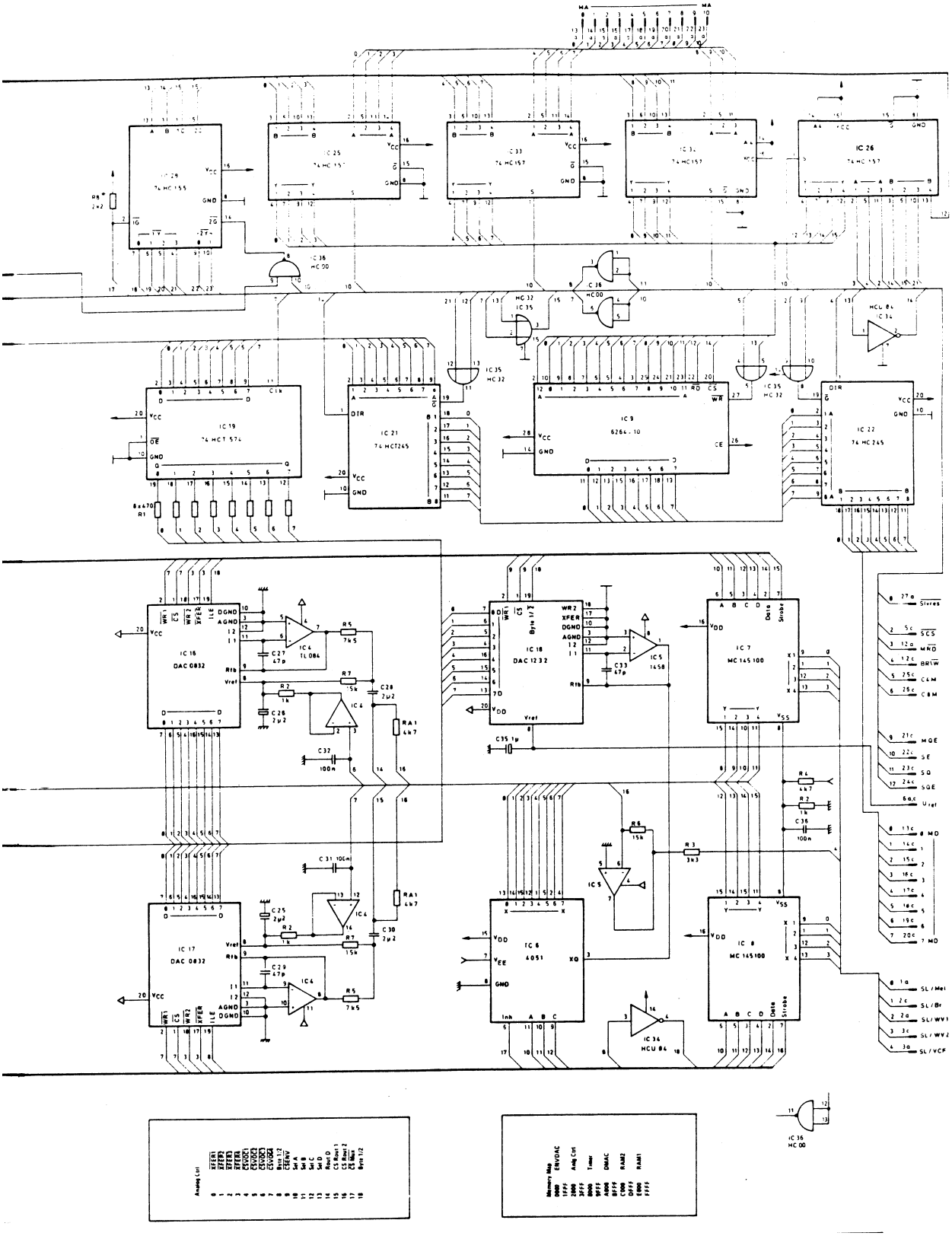
The crosspoint matrix (IC 7, 8, MC145100) causes the audio signals to be fed through to one of the five slave channels.



5L5, Component layout



SL5, Schematic diagram



4. CO1 (Co-Master)

The CPU 68B09E (IC 14) communicates with the master with the help of a "2-Port-RAM", as is known from the slaves 5L5. This means that the CPU is timed with SE and SQ, the inverse E and 0 of the master. Switching over between the master and co-master addresses or control signals is done by IC 16, 18, 20, 22 (HC 157) and PAL (IC 6), while IC 15 (HCT245) and IC 21 (HC245) switch over the data buses.

The RAM has a size of 64 kbyte and is in case of a power failure - similar to the MST8 board - protected against data loss. Since the CPU has an address size of 64 k only, but has to manage 192 kbyte of data and program, a large portion can be accessed to by banking. This is done by the bank latch 1C7 (HC174) in combination with the PAL (IC 6).

256 bytes from the 32 k program area are for I&O (IC 1, IC 2). IC 3 (HC138) is responsible for decoding in the I/O area.

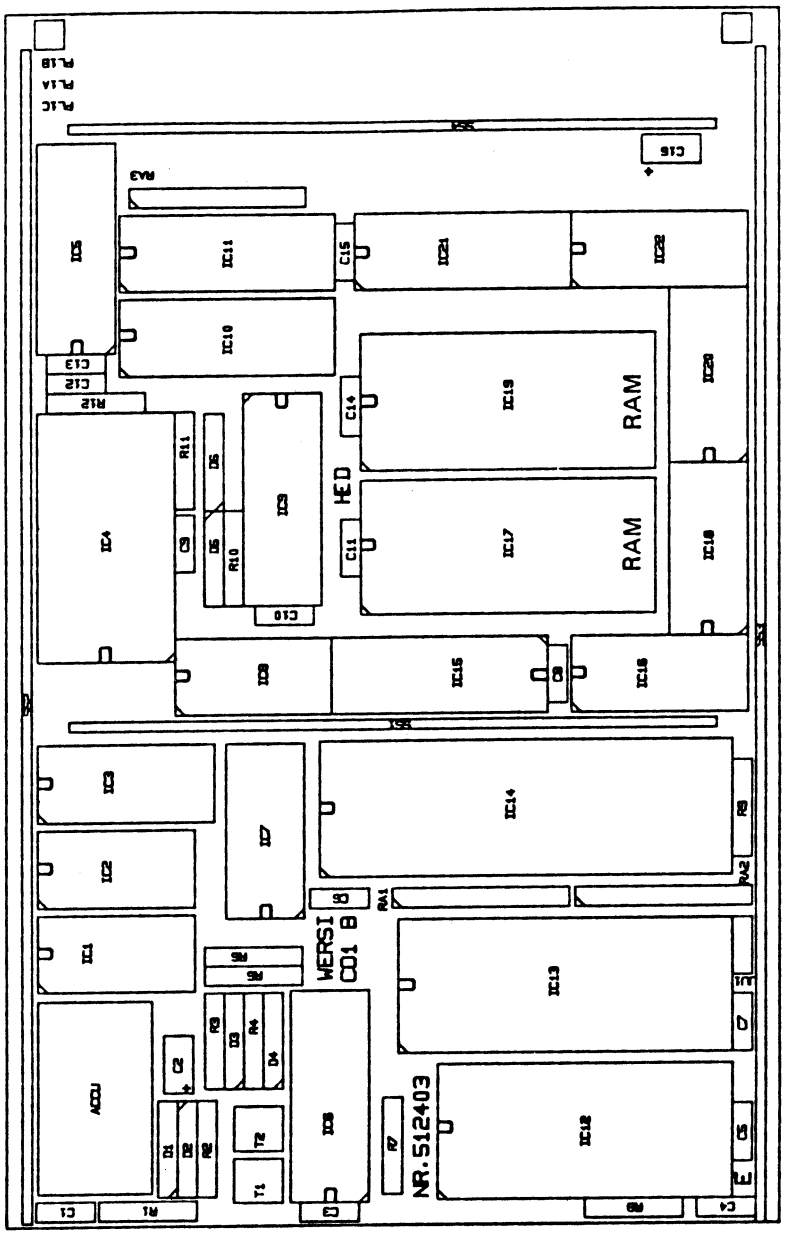
The timer (IC 12) produces the necessary interrupts for the system software and the clock for the ACIA (IC 4).

The ACIA is the serial interface of the organ and provides or processes the serial data flow of the MIDI interface or the R5232 interface.

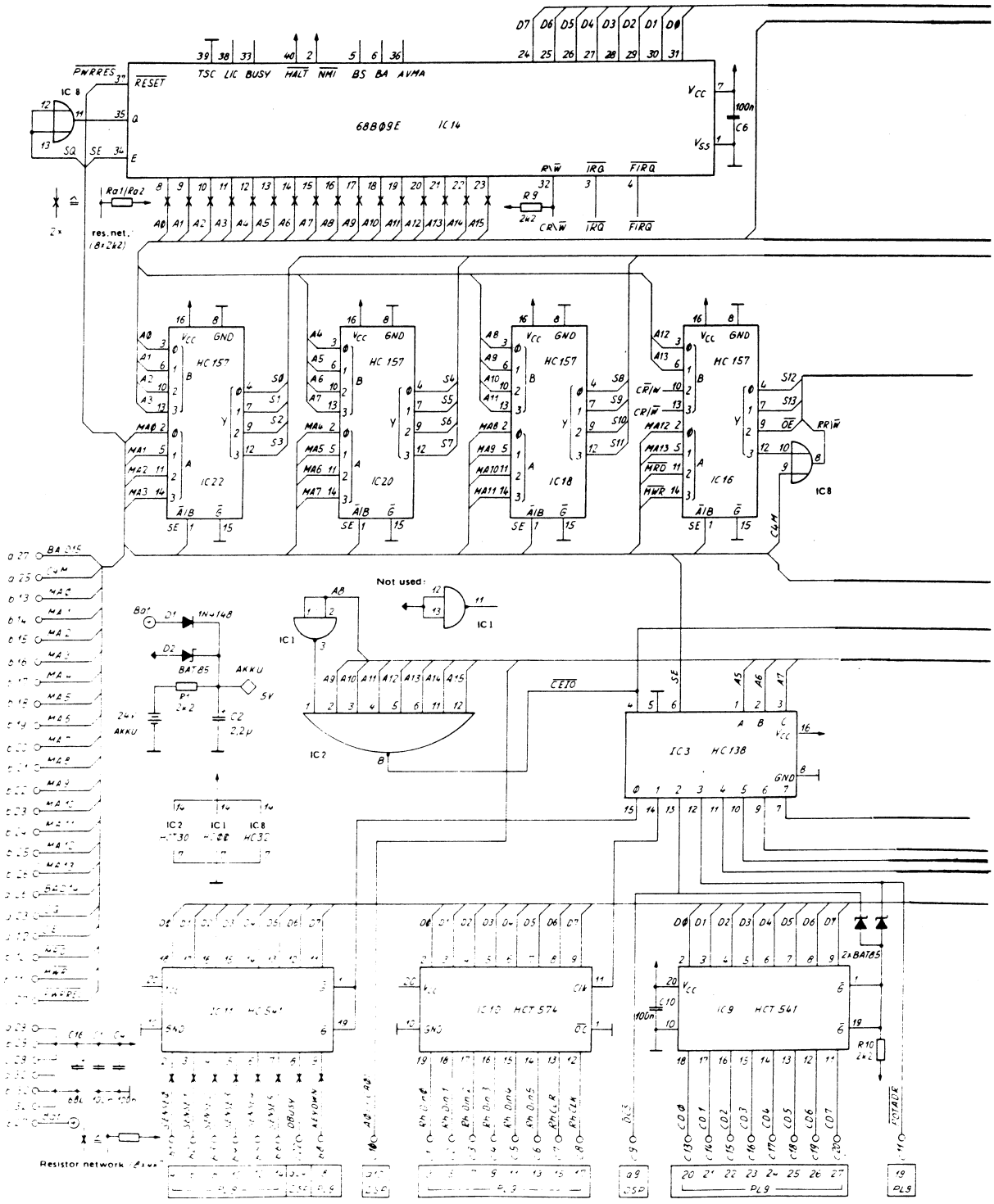
The ADCO804 (IC 5) converts the voltage values coming from CB 40 (volume control board) into digital values.

IC 10 (HCT574) and IC 11 (HC541) are responsible for the operation of the rhythm control panel.

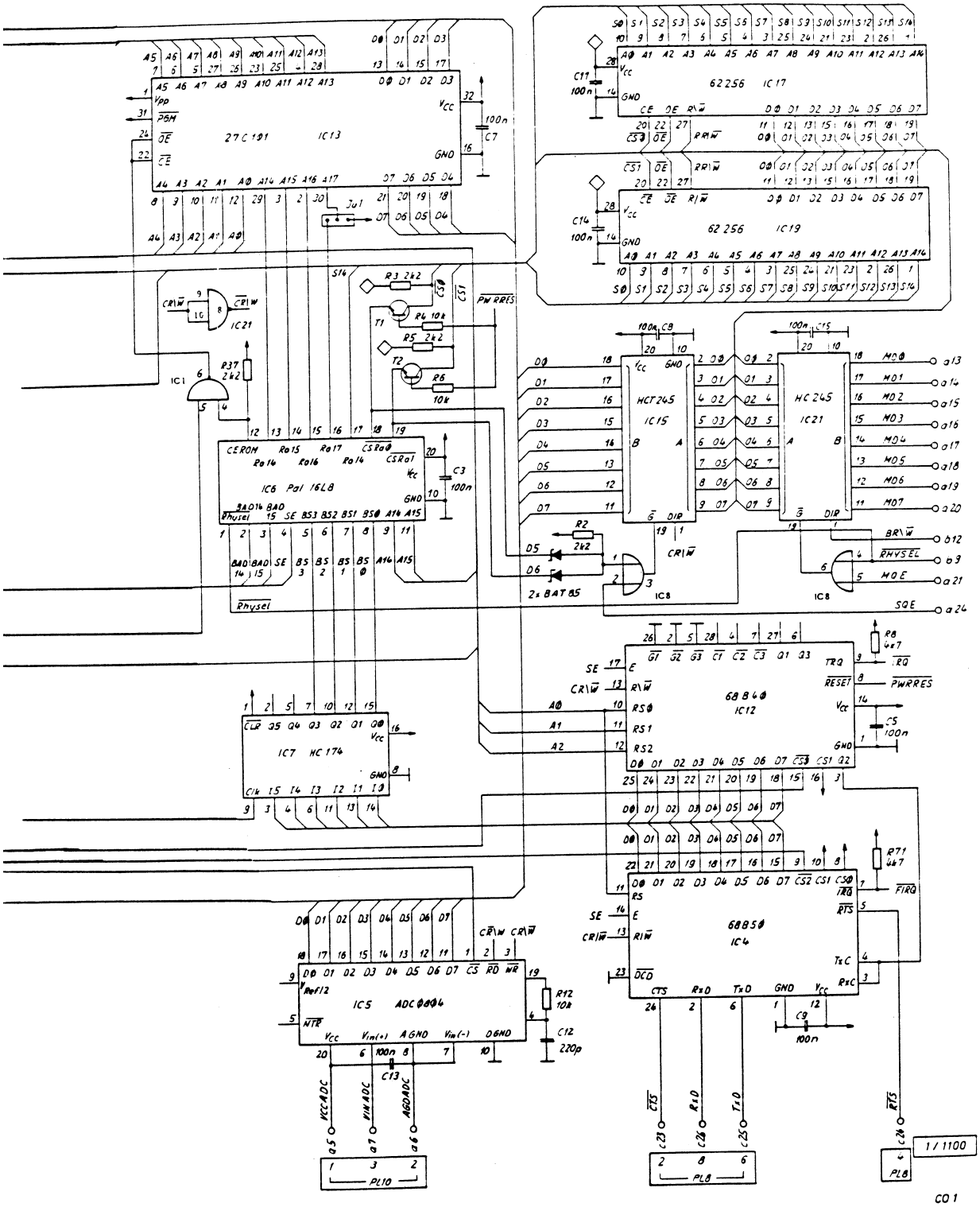
Via IC 9 (HCT541), data is transferred (DCS) to the drums (DSP 160) or the potentiometer address is written into the latch on CB4O (POTADR).



C0l, Component layout



C0l, Schematic diagram

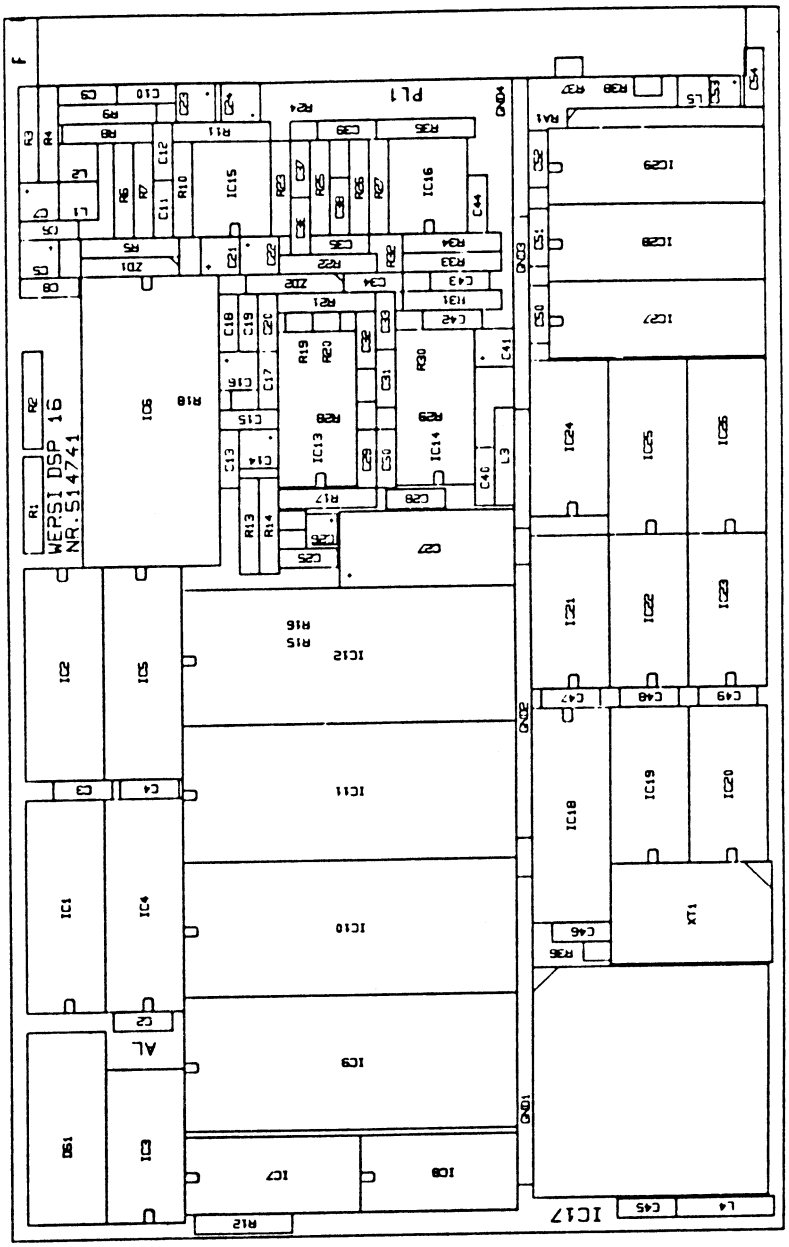

27C101 IC13
62256 IC17
62256 IC19
HCT245 IC15
HC245 IC21
CEROM PAL 16L8 IC6
HC174 IC7
68B40 IC12
68B50 IC4
ADC0804 IC5
2x BAT85
1/1100
CO1

5. DSP 160 (Drums)

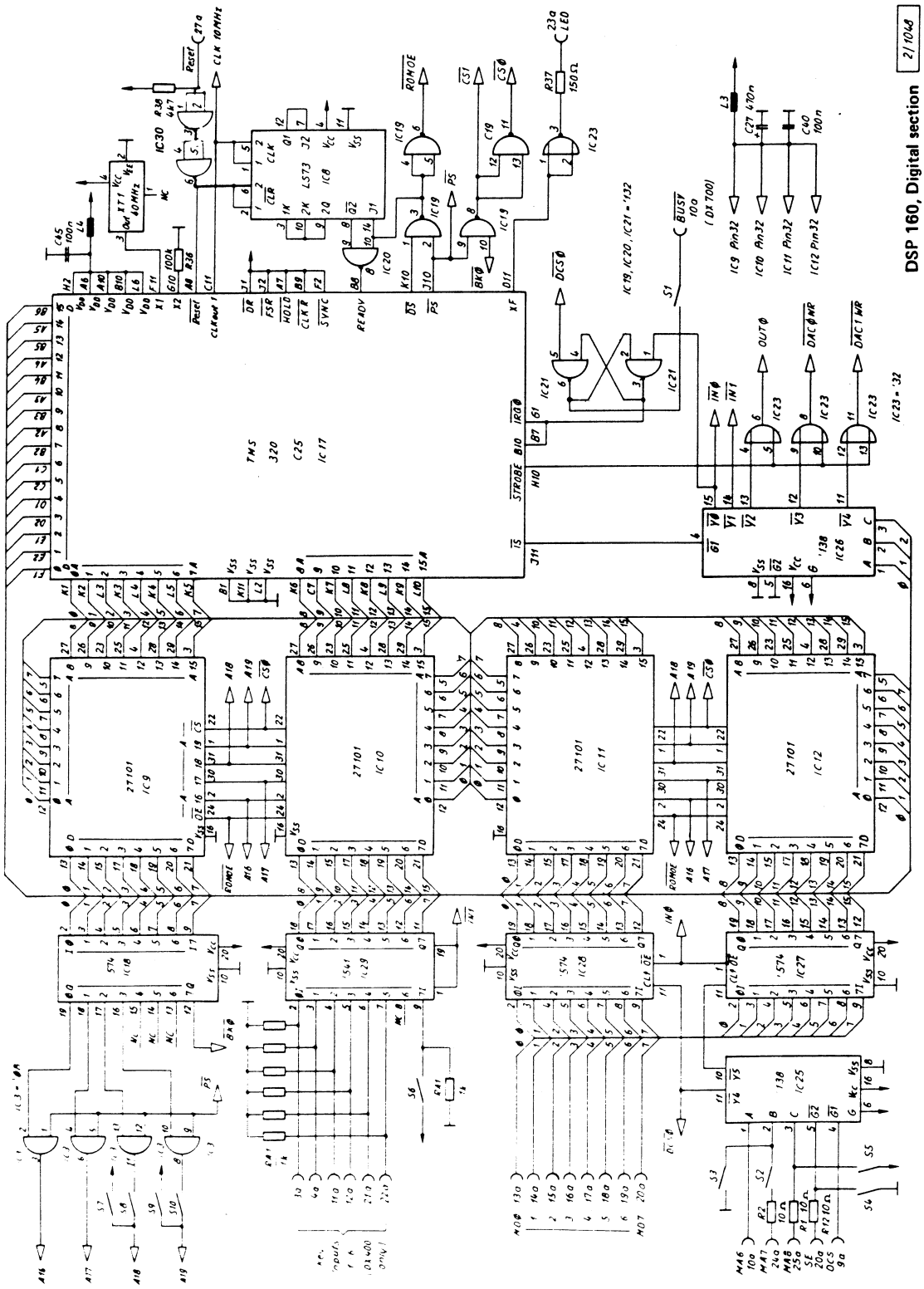
The PC Board DSP 160 carries the complete drums with all its instruments like bass drums, snare drums, Hihat, etc. The drum instruments were digitally recorded in a studio. This means, each instrument sound was converted into digital information to be stored in integrated semi-conductor memories. The contents of these semiconductor memories can be - following a certain process - converted into audible sounds as often as required. Cs 9, 10, 11 and 12 on PC Board DSP 160 are such semi-conductor memories. Reading out these memories (basically, "replaying" the "recorded" sounds) is done by the signal processor IC 17 (CPU). This processor, together with the ICs 9, 10, 11, 12 (=data storage), is a complete 16 bit-computer with internal 32-bit-data processing. One interface to the outside world is the 16-bit Input Port IC 27/IC 28, which receives the drums trigger signals sent to the DSP 160 from the organ. These trigger signals determine which drum instrument is to be started as well as its volume level.

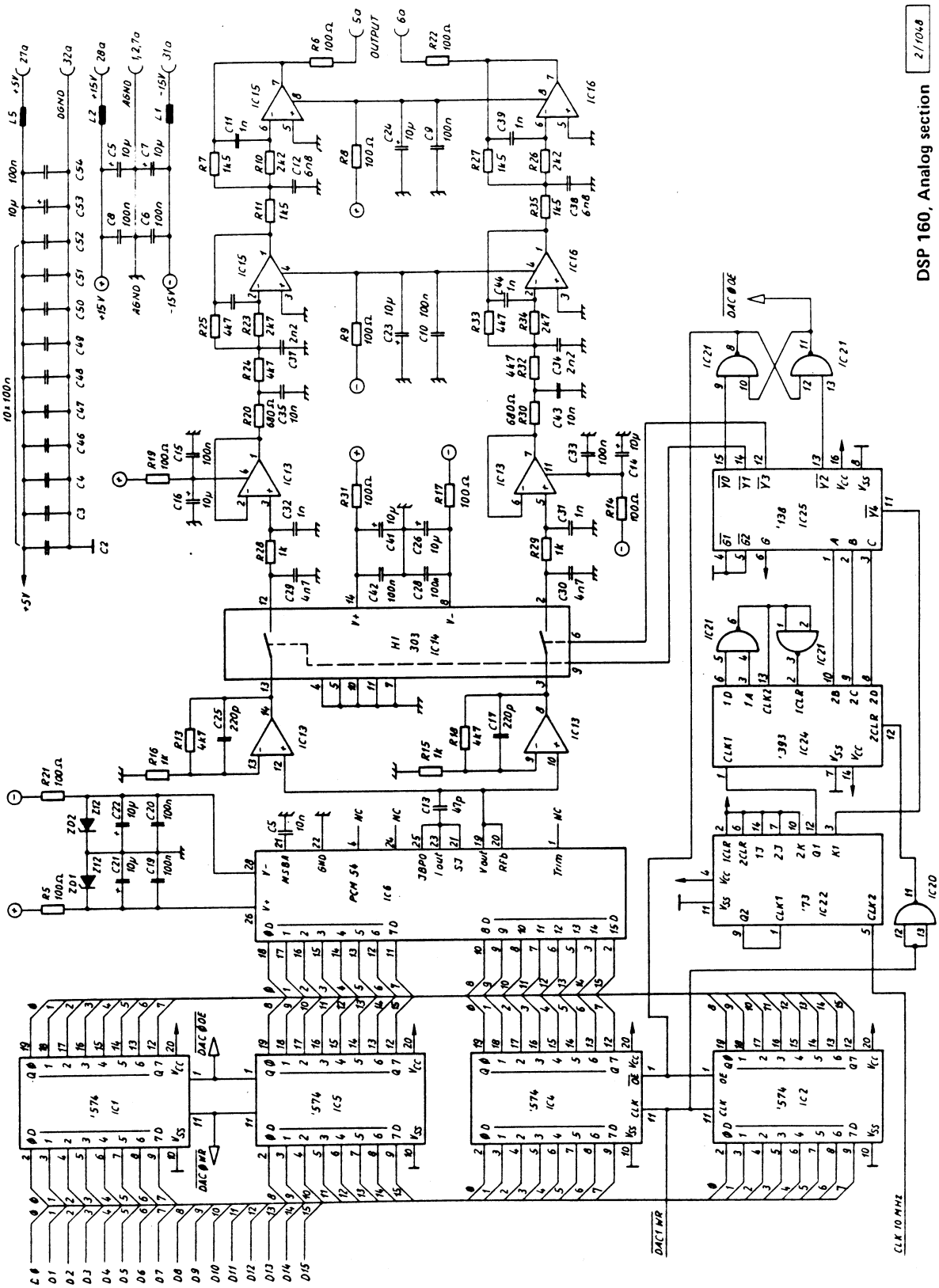
The second interface to the outside is the digital-analog-converter IC 6, which is connected to the CPU via the latches IC 1, 2, 4, and 5. The DIA converter converts the digital drum sounds into audible analog signals with a resolution of 16-bit (65535 steps of resolution, similar to compact disks).

The analog switch IC 14 which follows the converter guarantees in combination with the sequence control IC 20, 21, 22, 24, 25 that the digital stereo signal at the input of latches IC 1, 2, 4, 5 is converted into a real audio 2-channel signal. This signal is routed separately for both channels via low-pass filters (IC 15 and IC 16), which filter out unwanted clock frequencies.



DSP 160, Component layout (Note: Layout shown is DSP 16, DSP 160 has an additional IC 30).


DSP 160, Digital section
2/1048


DSP 160, Analog section
2/1048

6. DH 11 (Digital Reverb Unit, 12 Bit)

The input signal (plug 1, pin 5) is applied to the input of IC 14 (NE 571), pin 6) via C 31.

C 31 serves for high-frequency emphasis.

With IC 14a and IC 16 a (TL 084) dynamics are compressed and levels are limited to maximum 5 Vss (D 7, D 8). The Iowpass filter following (IC 16b, c, d) serves as band limiter (4 kHz: approximate -60 dB).

Now that frequency response and dynamics are adjusted to the digitalization process, the signal is kept on a constant amplitude value by IC 13 (LF 398, Sample & Hold) during the necessary conversion time required by the analog-digital-converter.

IC 11 translates the analog signal into a 12-bit code. This code is split up into 2 bytes that are fed through to the CPU (IC 1, 68B09) one after the other by IC 5 and IC 6 (74 LS 244).

The CPU is controlled by the program (short and long reverb, fast and slow echo) stored in IC 2 (2k EPROM).

From the CPU, the digital information (data) is placed into memory (IC 7, 8k RAM), read out with time delay, added to other data, saved again, etc.

The frequency of this process caused by the 12-bit code of the ADC results in reverb times of up to 4 seconds; CPU and RAM have a bandwidth of 16-bit.

The complete signal (12-bit again) is again split up into 2 bytes and routed to the digital-analog-converter (DAC 1230, IC 12). This converter produces an output current, which represents the digital value.

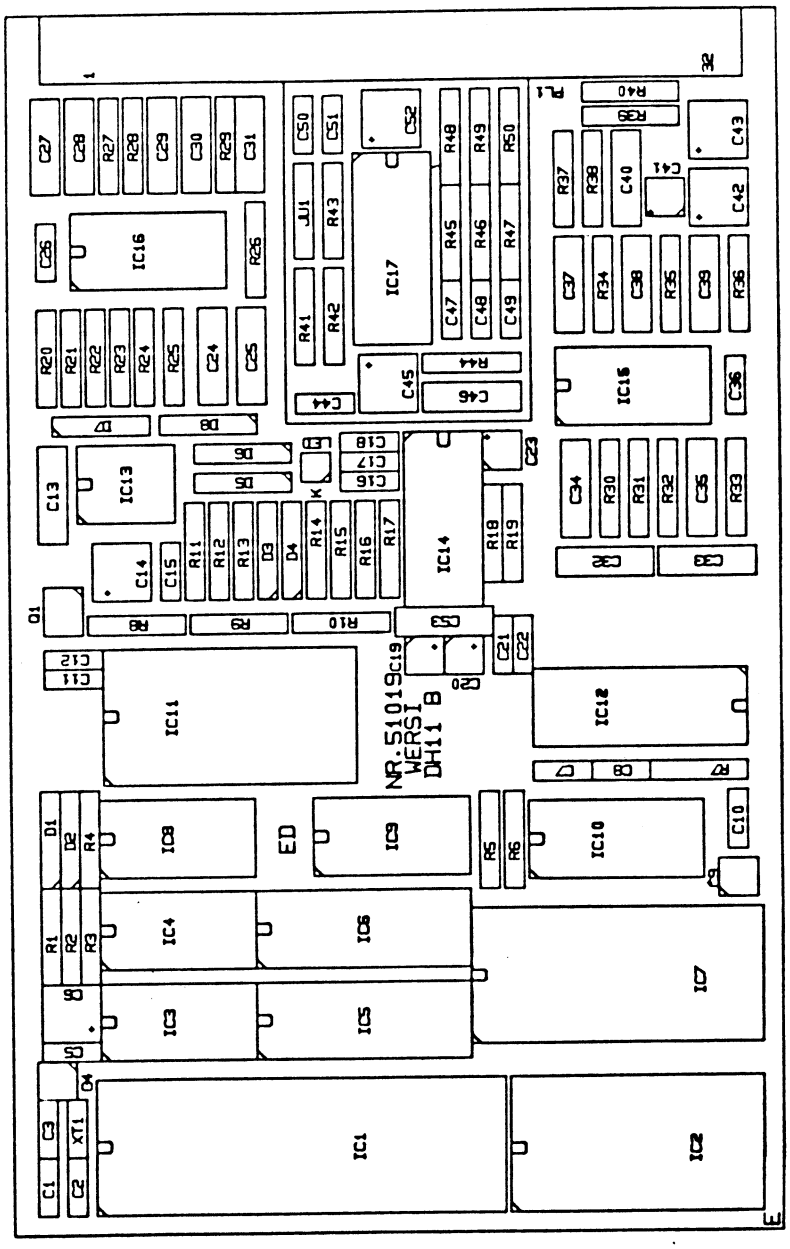
This current is converted into a voltage potential by IC lSc (TL 084), which still has amplitude jumps and unwanted frequency portions, due to the previous digitalization process.

The following low-pass filter (IC 1Sa, b, d) smoothes the signal, i.e., filters out the disturbing portions. C 40 and IC 14b reverse the high-frequency emphasis and the dynamics limiting process described in the beginning.

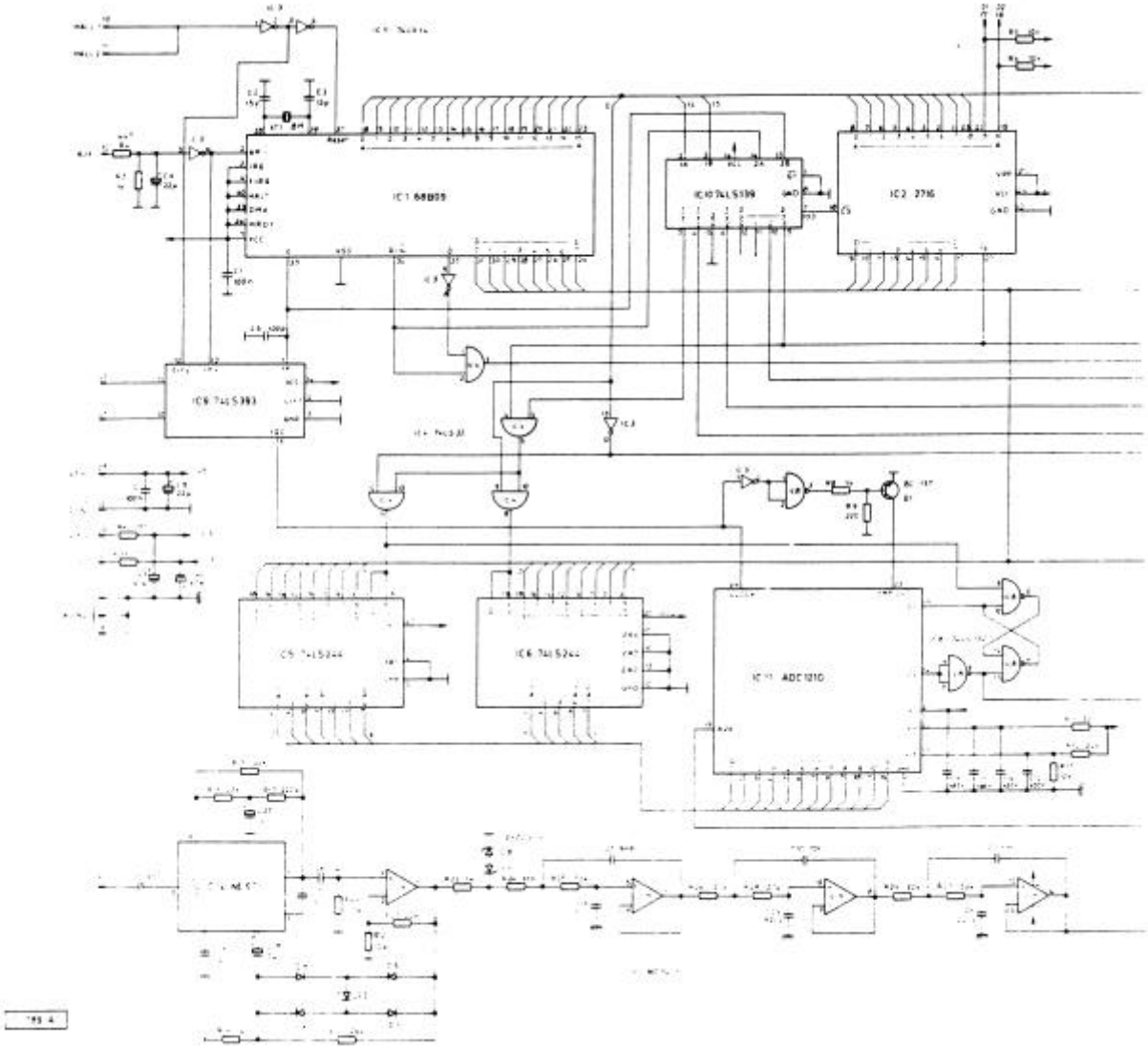
The reverberated and delayed output signal is applied either to pin 6 (single-channel operation) via JU 1 or is doubled by IC 17 (TDA381O) so that a second "stereo" channel is produced. By means of exactly determined phase rotations in certain areas of the frequency range, this IC generates a second output channel (pin 9). Further stereo processing of the two channels produces proper stereo imaging.

Switching over between the various operation modes (short and long reverb, fast and slow delay) is done by the NM of the CPU by sending pulses to pin 12.

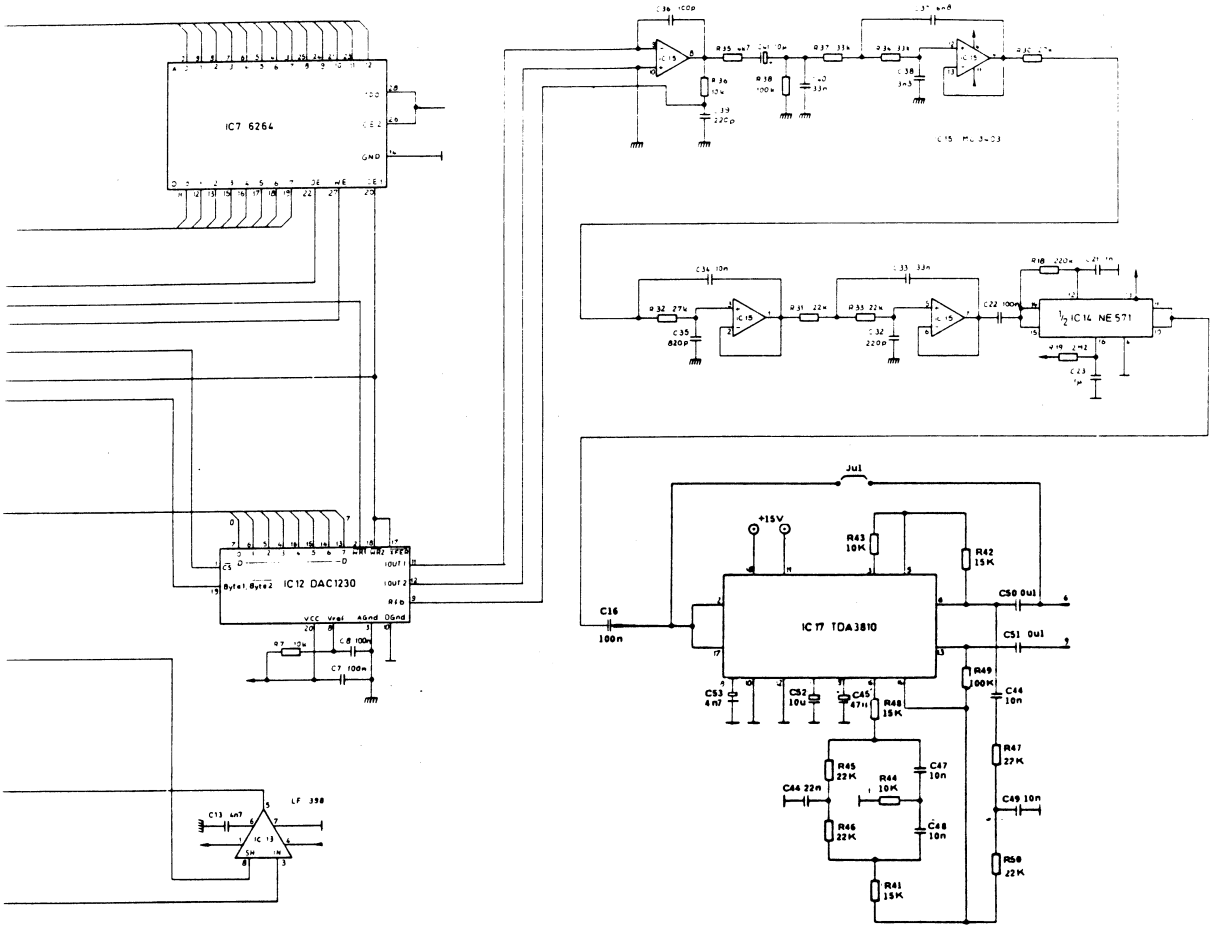
Reset activates the program sequence.



DH11, Component layout



DH 11, Schematic diagram


IC7 6264
IC12 DAC1230
IC 17 TDA3810
+15V
C16
100n
R43
10K
R42
15K
C50 Out
C51 Out
R49
100K
C44
10n
R47
27K
C49 10n
R50
22K
R41
15K
C53
4n7
C52
10u
C45
47u
R48
15K
R45
22K
R44
10K
C47
10n
C44 22n
R46
22K
C48
10n
LF 398
IC 13
C13 4n7
1/2 IC14 NE 571

7. DH 100 (Digital Reverb Unit, 16 Bit)

Basically, the digital reverb unit DH 100 consists of two sections:

1. digital section

2. analog section.

The digital section is a complete 16-bit computer consisting of a 16-bit CPU with 32-bit internal data processing (IC 4), the program memory (IC 1 & IC 5) and the data storage IC 2/IC 3.

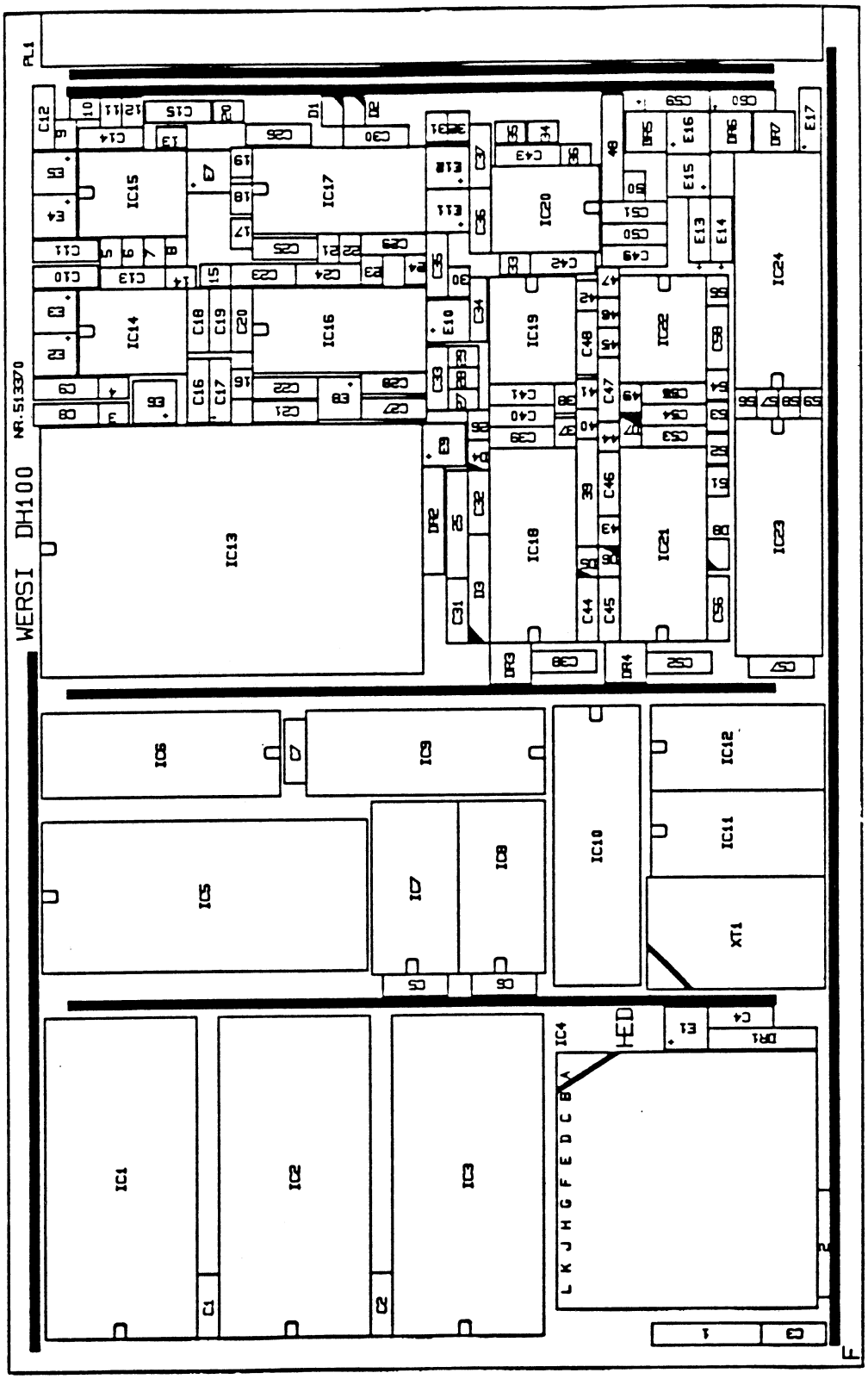
The processing rate of the CPU is determined by the master clock oscillator XT 1. The XT 1 produces a clock signal of 40 MHz which is divided by 4 in the CPU IC 4 and results in the bus frequency 10 MHz = 100 ns instruction cycle time.

The analog signal to be reverberated, which is assigned, to pin 5 of plug 1 is amplified and routed to the analog switch IC 16 via a 6-stage lowpass filter. The analog switch guarantees that the input signal is kept at a constant level while the AID converter IC 13 converts the analog signal into digital information. The converter translates the analog input signal *(+1-10* volt) into a digital value with a resolution of 65535 steps. With a sampling rate of 28 kHz, this value is sent to the CPU IC 4 via the input latches IC 6 and IC 9.

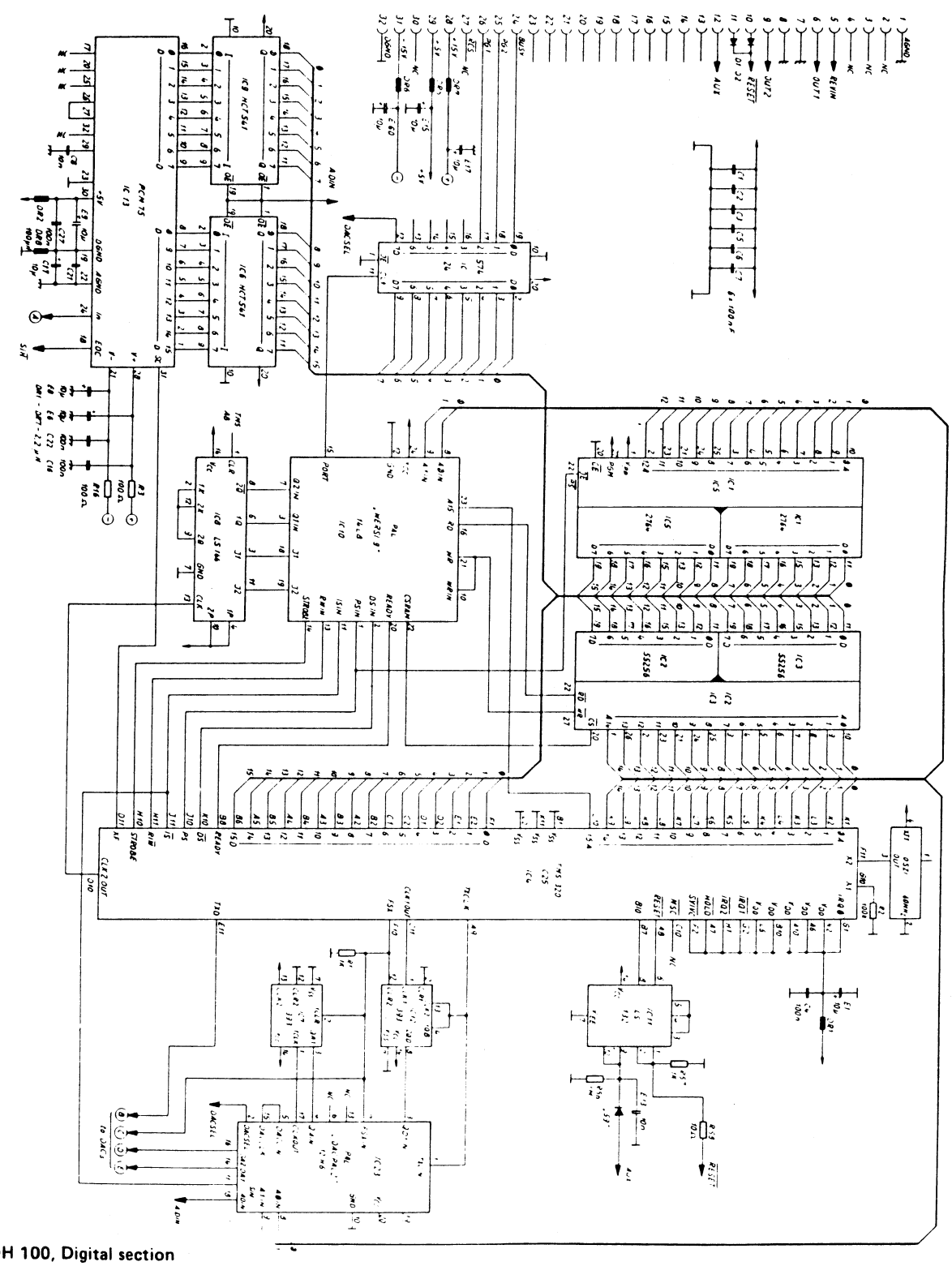
After processing (computing the reverb) the digital stereo signal generated in IC 4 is led to the second interface (output), back to the analog section: the two digital-analog-converters IC 18 and IC 21. These, again, generate analog signal from the digital information, the clock frequency portions of which are filtered out by Iowpass filters.

Now the reverberated stereo signal can be received at the outputs of IC 20.

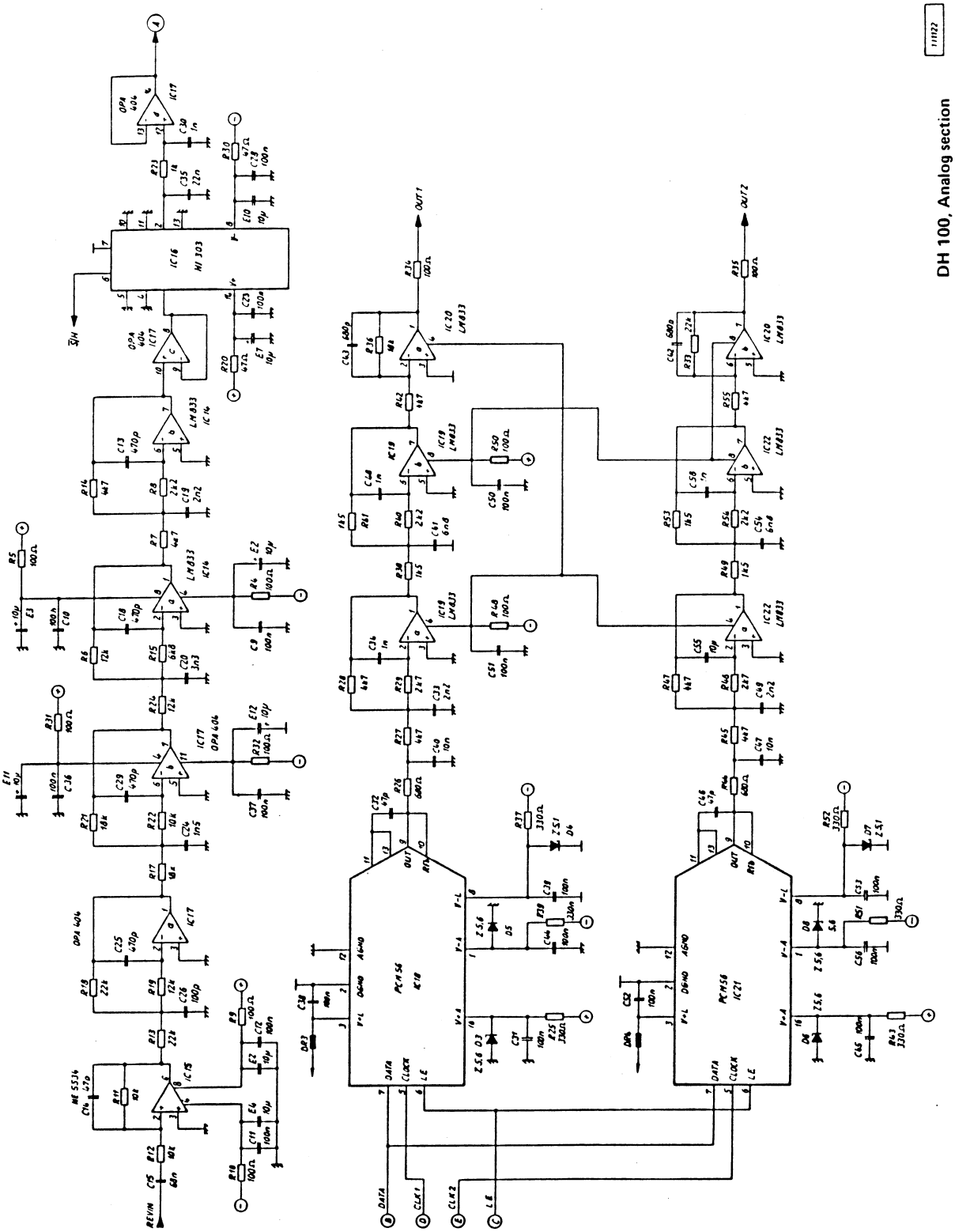
IC 8 and IC 10 guarantee exact timing of the read/write signals for the storage ICs. IC 7, IC 12 and IC 23 produce the control signals for the two digital-analog converters.



DH 100, Component layout



DH 100, Digital section



DH 100, Analog section

8. IF 40 (Analog and Digital Control)

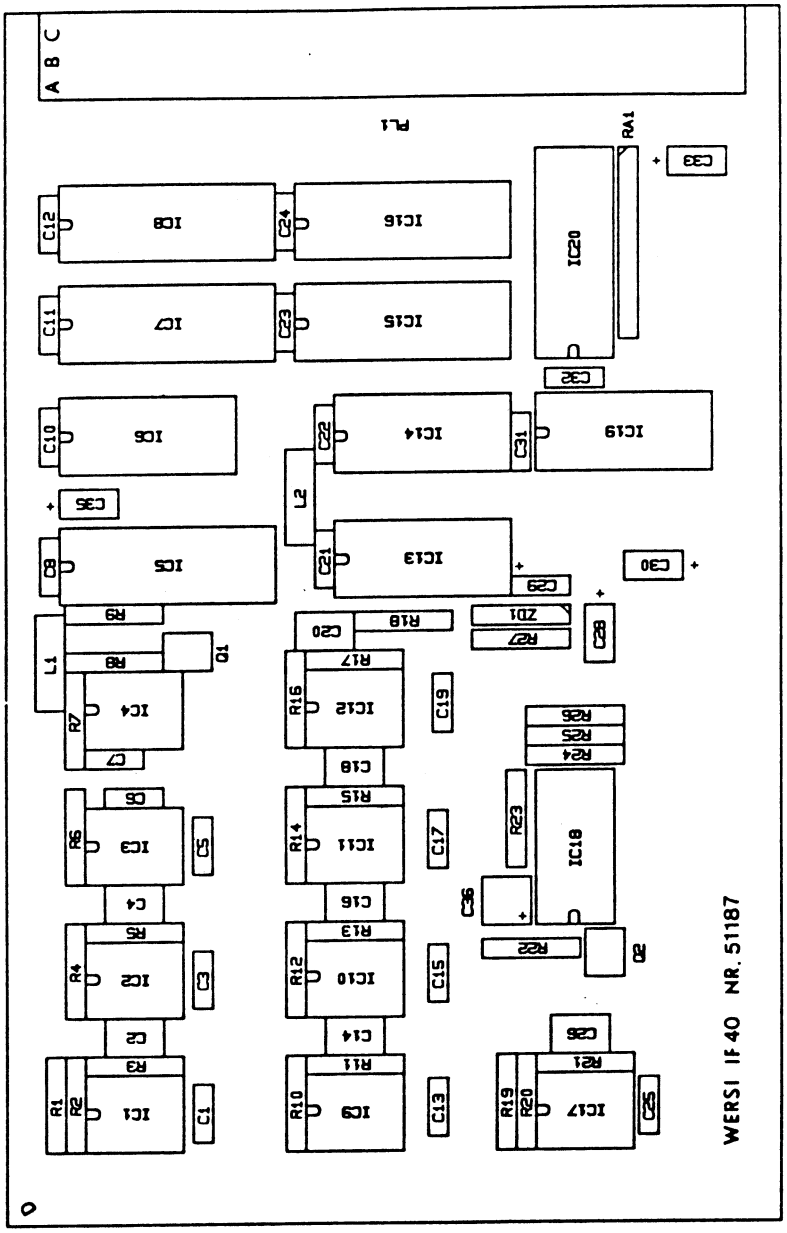
On this board the master data bus reaches its end. Here, all control signals and voltages are produced with which the master controls the audio routing, the Wersivoice settings, volume levels, etc.

The digital information for the control v6ltages is applied to the inputs of the DAC 0832 (IC 5) in multiplexed digital form and are converted into a corresponding voltage potential. This voltage potential is routed to the correct output by the de-multiplexer IC 13 (4051) which is controlled by IC 14 (HC 174), is stored in a Sample & Hold and adjusted to the correct voltage level.

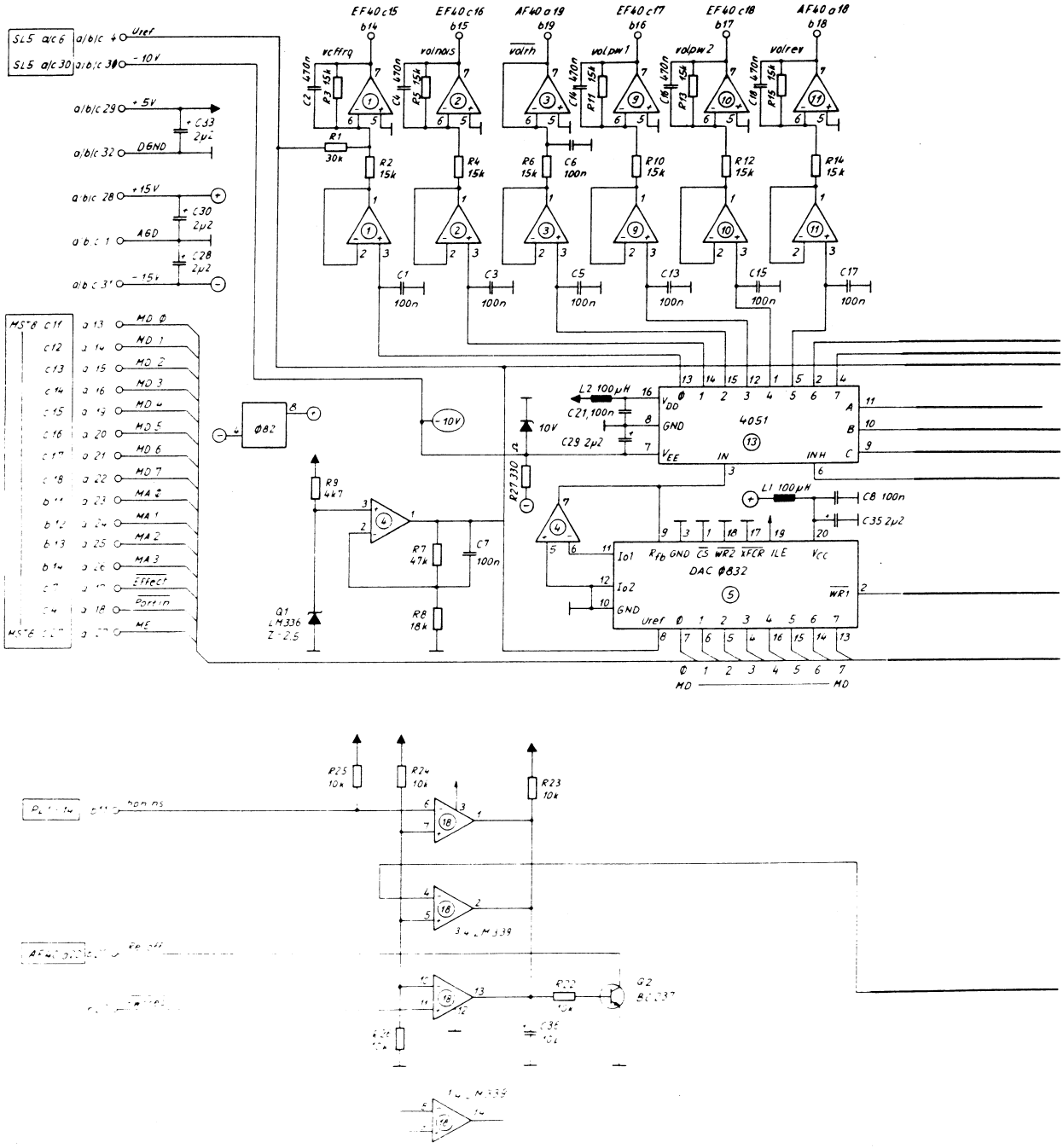
The remaining board consists of 5 output ports (IC 6-IC 8, IC 15 and IC 16) which generate the control signals, as well as an input port IC 20.

Q2 switches off the audio relay on AF 40 if..

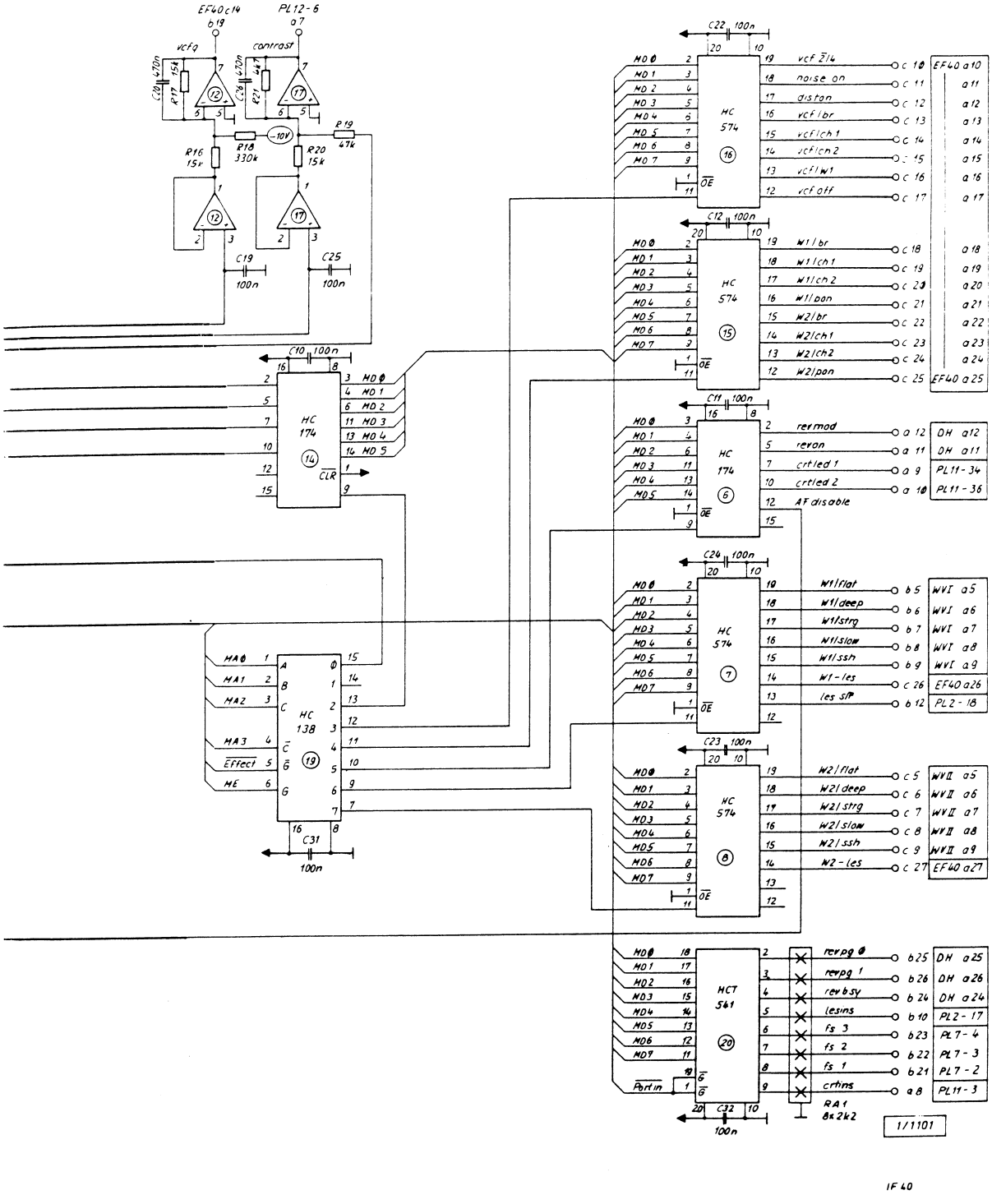
a) headphones are inserted (HPH INS)
b) reset is activated (PWRR ES)
c) the master switches off the relay (AFdisable).



IF 40, Component layout



IF 40, Schematic diagram


EF40 c14 b19
PL12-6 a7
vcfq
contrast
-10V
HC 574
HC 174
HC 138
HCT 541
vcf 3/4
noise on
distan
vcf lbr
vcf lch1
vcf lch2
vcf lw1
vcf off
w1/br
w1/ch1
w1/ch2
w1/pan
w2/br
w2/ch1
w2/ch2
w2/pan
rev mod
revon
crt led 1
crt led 2
AF disable
w1/flat
w1/deep
w1/strg
w1/slow
w1/ssh
w1-les
les s/p
w2/flat
w2/deep
w2/strg
w2/slow
w2/ssh
w2-les
revpg 0
revpg 1
rev bsy
lesins
fs 3
fs 2
fs 1
crtins
Portin
RA1 8x2k2
1/1101
IF 40

9. EF 40 (Effects and Routing)

On this board the 5 slave channels Bright, Mellow, WV 1, WV 2 and VCF are collected and amplified.

The Mellow-channel (Bright off) is routed directly via IC 5 to the two summing OPAMPs (IC 9) after cutting off its higher frequencies. Nearly the same is done with the Bright-channel; however, the cut-off frequency of this lowpass filter (IC 4) is higher than the one of the Mellow-channel. Also, the Mellow-channeI is distributed evenly to the left (Organ 1) and the right (Organ 2) channels via R 56 and R 57, while the Bright-channel is louder on the right channel than the left one via R SB and R 62.

The two Wersivoice stages are identical:

By two switches in the input stage the WV channel can be switched to Bright. If desired, you can add some noise with T 3 and IC 12 (or T 4 and IC 11 respectively); the envelope of the noise is determined by the control voltages VOLPW1 or VOLPW2.

In the case of WV1, the VCF signal may also be added via R 14/C 69.

With the switch (IC B and IC 7) following the OPAMP (IC 3 and IC 2) the WV signal can be routed to an external Leslie (W1 -LES, W2-LES) or the PC Board WV 30.

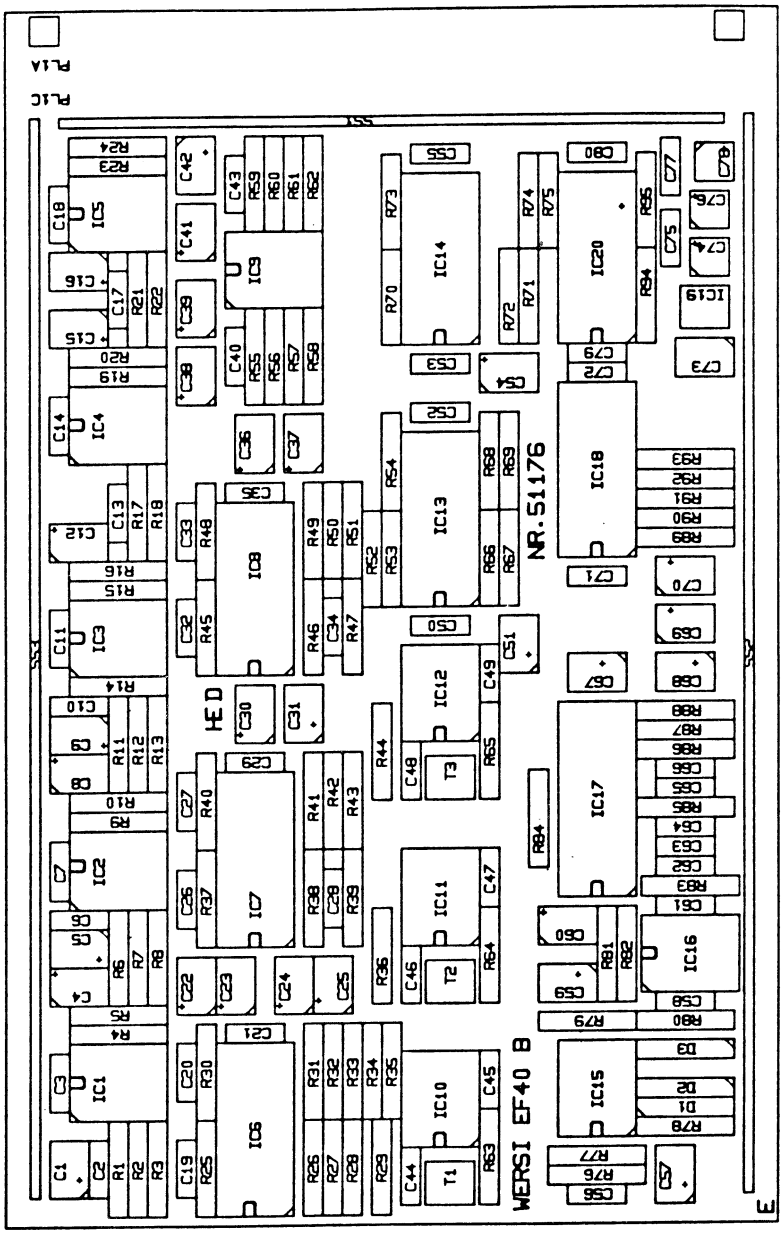
The output signal of the Wersivoice which is present at pin C 4 or pin C 5 of plug PL 1 is routed individually to the organ channels left and right with the switches IC 13 or IC 14.

The VCF channel from the slaves can be switched with Bright on or off via analog switch IC 6 by control VCF/BR. It can also be switched via IC 6 by DISTON to the distortion stage IC 15, or directly to the VCF module (IC 17) via IC 1 and C 1. When the latter is the case, noise can also be added by IC 10 via T 1.

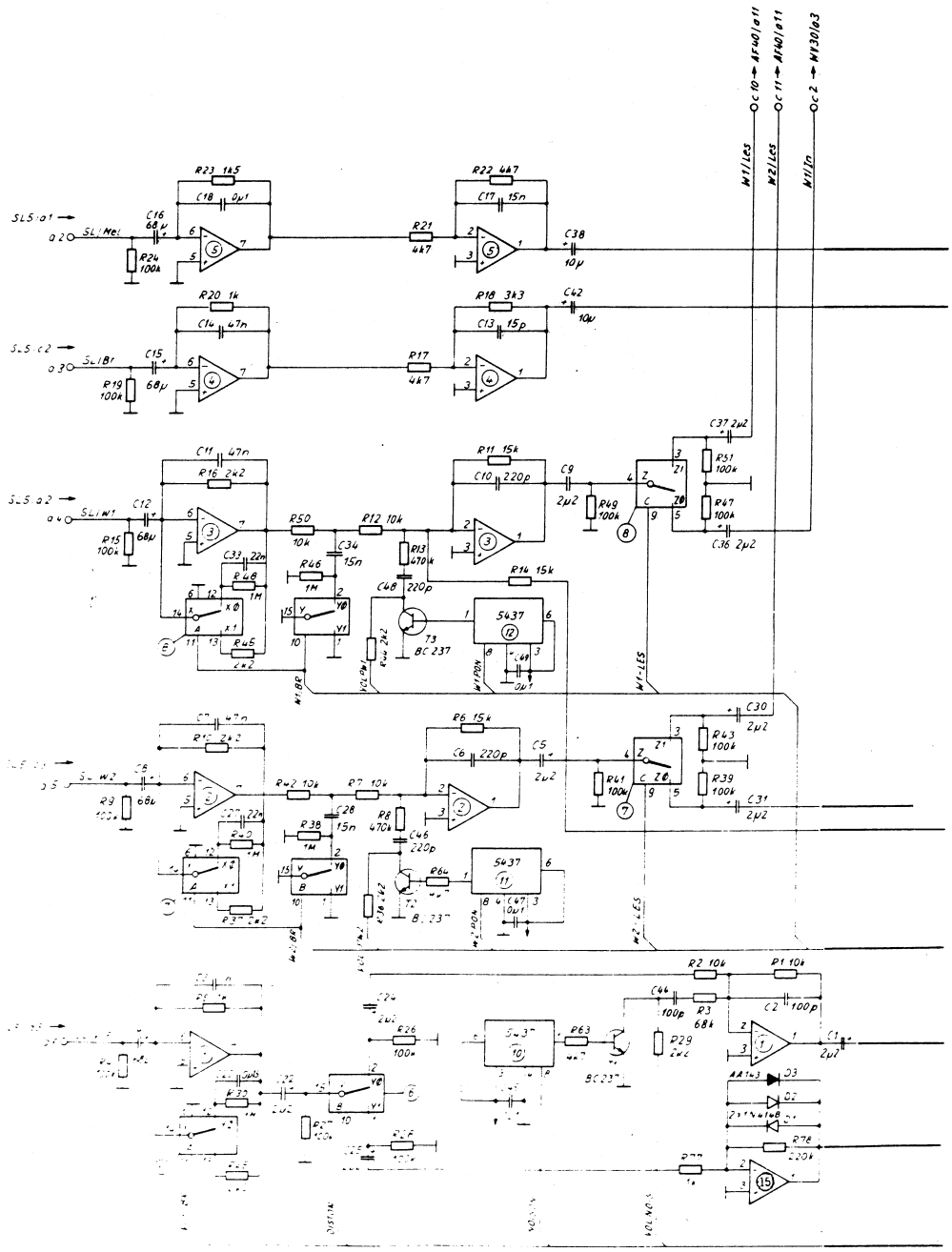
The quality and frequency of the VCF IC SSM 2045 (IC 17) is adjusted with the control voltages VCF/F and VCF/Q.

The VCF is equipped with a 2-pole filter and a 4-pole filter output, which can be selected with switch IC 18.

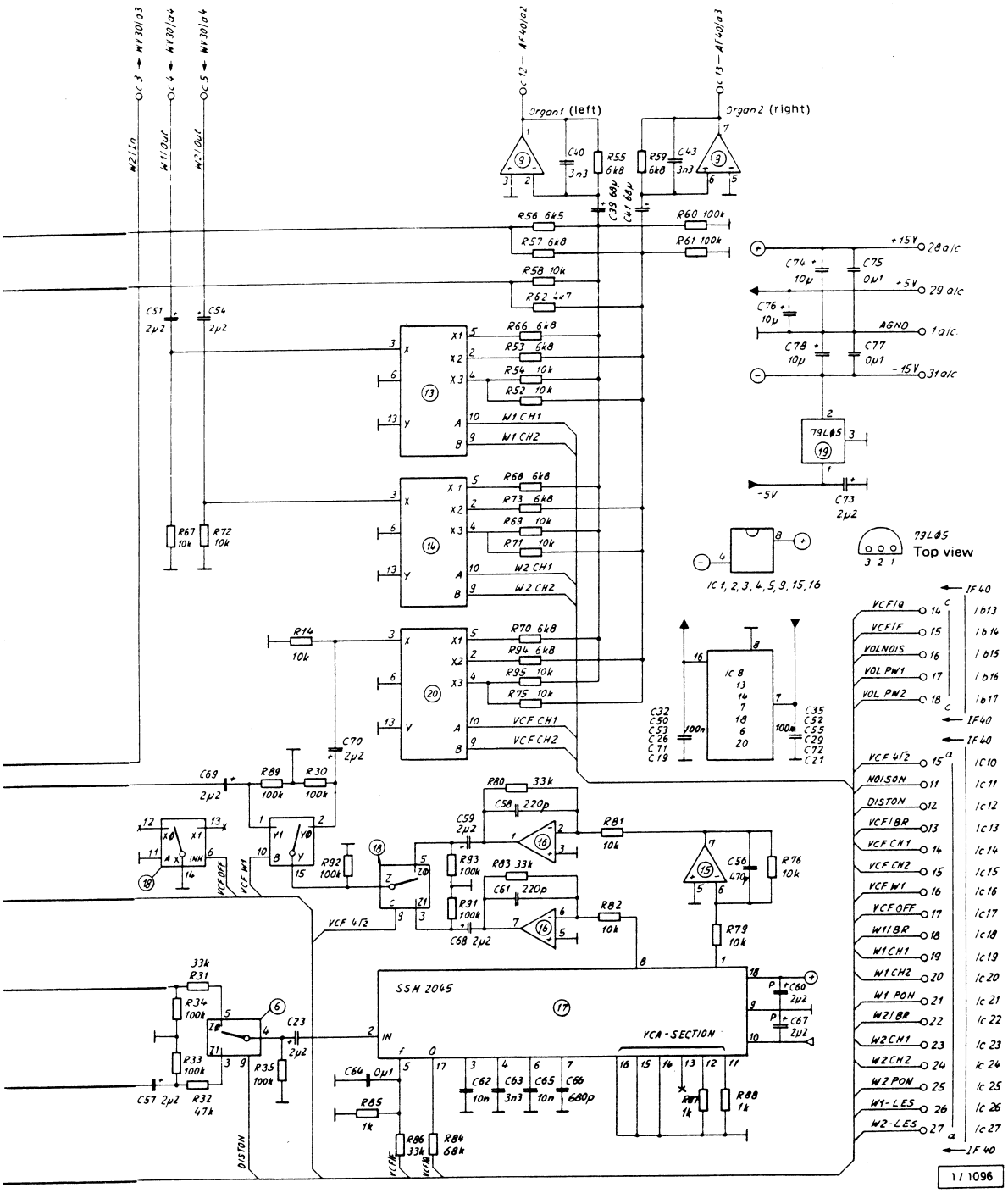
Then you have the possibility of routing the VCF signal to the channel switch IC 20 or to WV 1; IC 20 will split up the signal for the left and right organ channels.



EF 40, Component layout



EF 40, Schematic diagram


Organ1 (left)
Organ2 (right)
SSM 2045
VCA-SECTION
+15V
+5V
AGND
-15V
79L05
Top view
IC 1, 2, 3, 4, 5, 9, 15, 16
IC 8
W1 CH1
W1 CH2
W2 CH1
W2 CH2
VCF CH1
VCF CH2
VCF 1a
VCF 1F
VOLNOIS
VOL PW1
VOL PW2
NOISON
DISTON
VCF 1BR
VCF CH1
VCF CH2
VCF W1
VCF OFF
W1 1BR
W1 CH1
W1 CH2
W1 PON
W2 1BR
W2 CH1
W2 CH2
W2 PON
W1-LES
W2-LES
IF 40
1 / 1096

10. WV 30 (Wersivoice)

Basically, the WV 30 board is a phase/frequency modulator, which is responsible for two effects: the "Strings" effect and the "Leslie" effect (simulating rotating speakers).

The modulation is produced by mixing differently delayed audio signals together. The delay is generated by special components, so-called bucket brigade devices. Bucket brigade devices delay a certain audio signal proportionally to a clock frequency.

The WV 30 employs three bucket brigade devices (block diagram: BBD 1-3). Each bucket brigade belongs to a voltage controlled oscillator (VCO 1-3). The VCOs are modulated by two LFOs (low-frequency oscillators) with three outputs each.

"Strings" effect: LFO 1 has a frequency of 0.6 Hz and generates three triangle voltage signals, which are displaced to each other by 1200. LFO 2 has a frequency of 6 Hz and generates three sine wave signals, which are also displaced to each other by 120°.

Rotation (Leslie) effect: LFO 1 has a frequency of either 0.6 or 6 Hz (vibrato fast/slow), LFO 2 is off.

The Deep and Flat switches are effective on the audio path. Deep being a feedback process (amplification of the respective effect) and Flat being a partial "short circuit" of the bucket brigades (smoothing the respective effect) -

The elements of the block diagram can easily be seen in the schematic diagram:

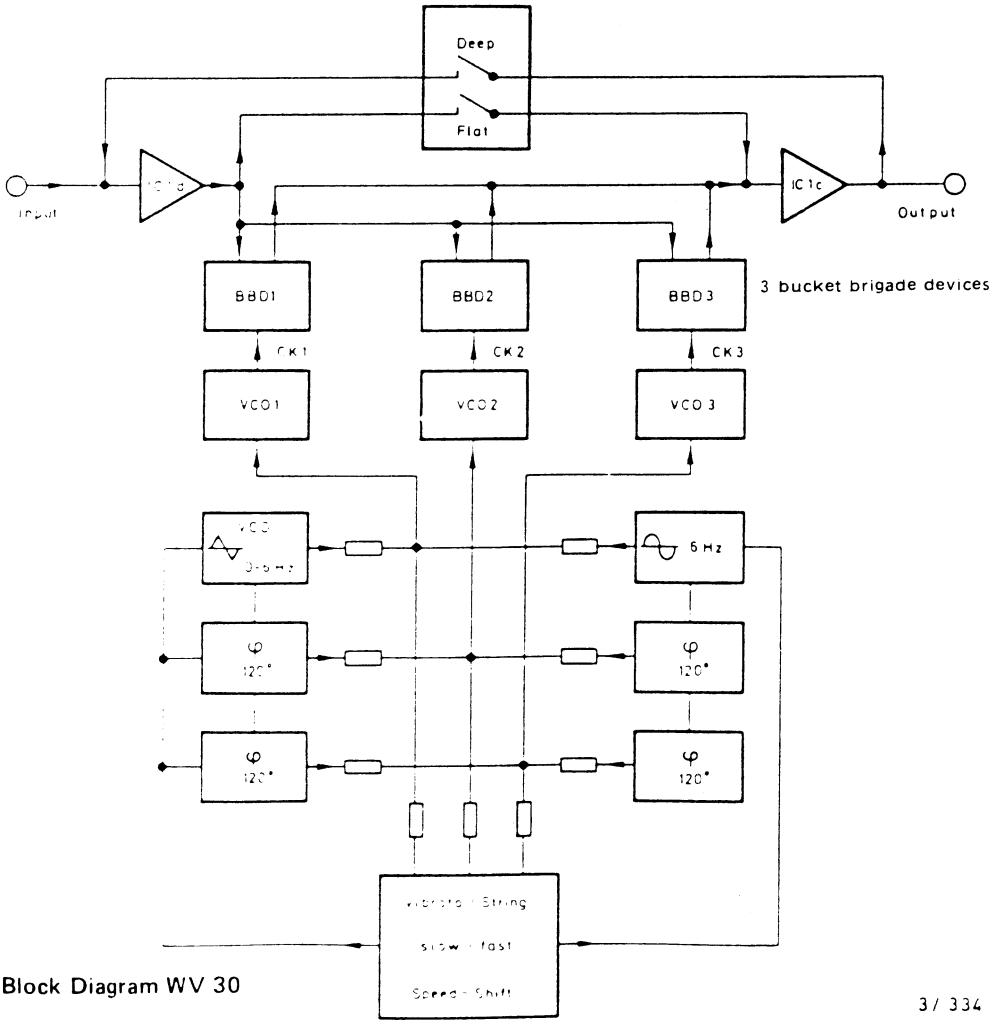
Via IC 2, the input signal reaches the bucket brigades (IC 4, 5,6). The corresponding VCOs consist of IC 7-9 and Q 3-8.

The LFO 1 consists of IC 11, 12, 13: LFO 2 consists of IC 10, 14.

The remaining three OPAMPs in IC 2 form the output filter amplifier.

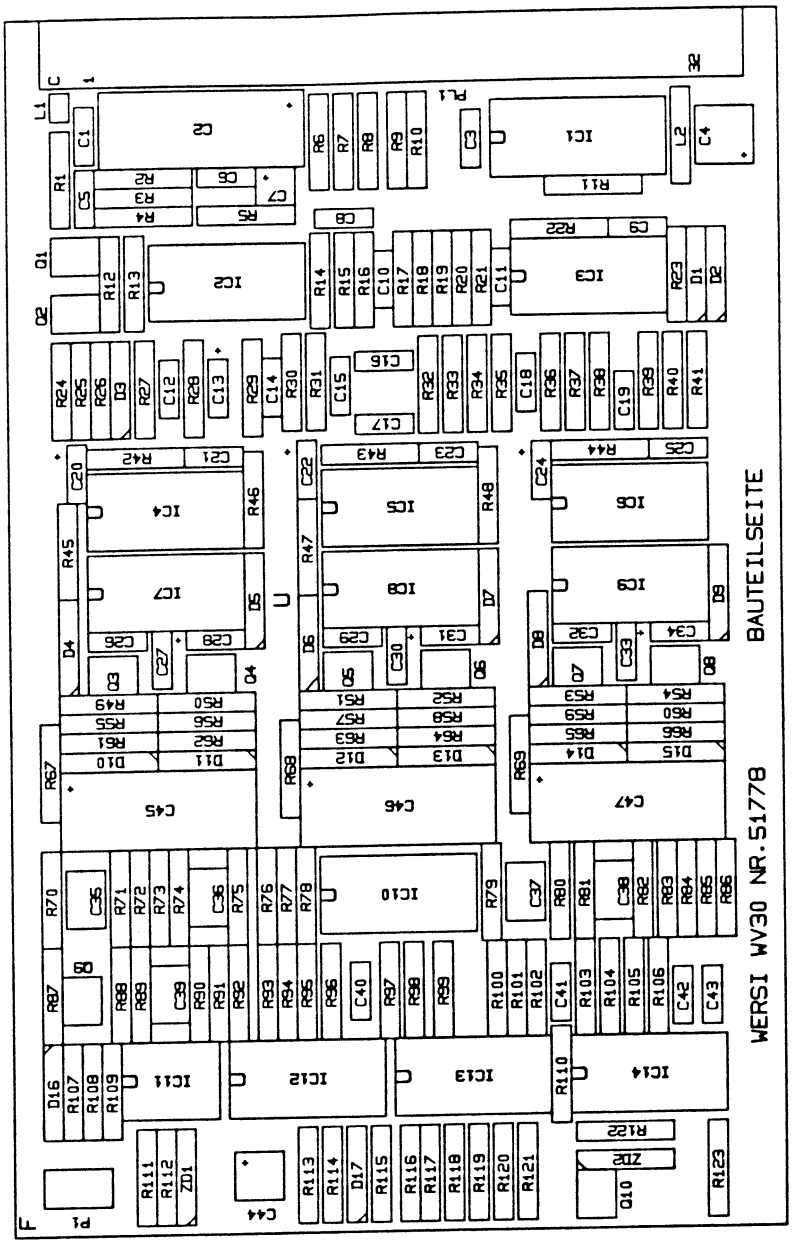
IC 3 is the switch to determine the feedback for the Deep/Flat effects.

IC 1 is responsible for the TT 1/CMOS level conversion.

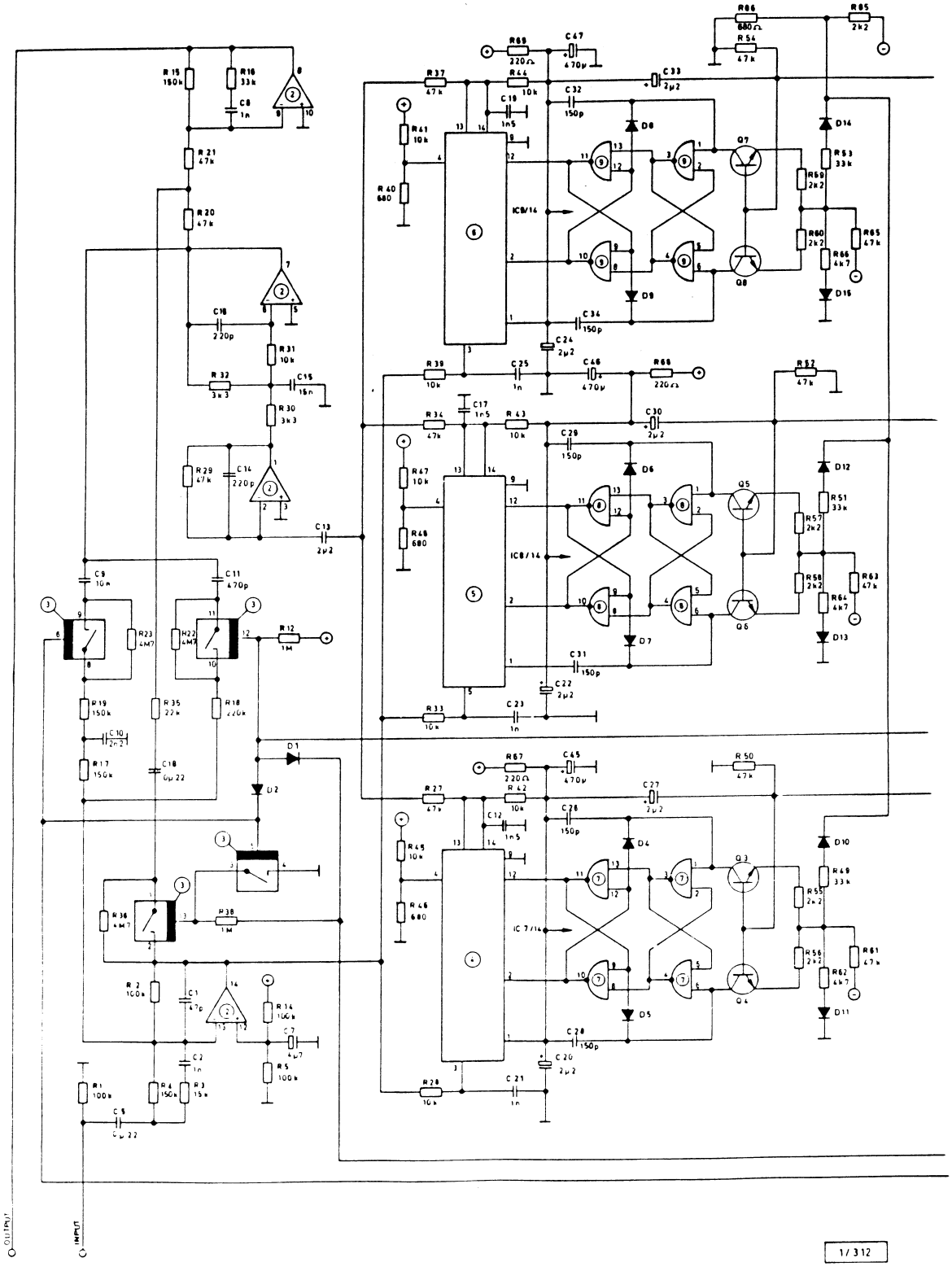


Block Diagram WV 30

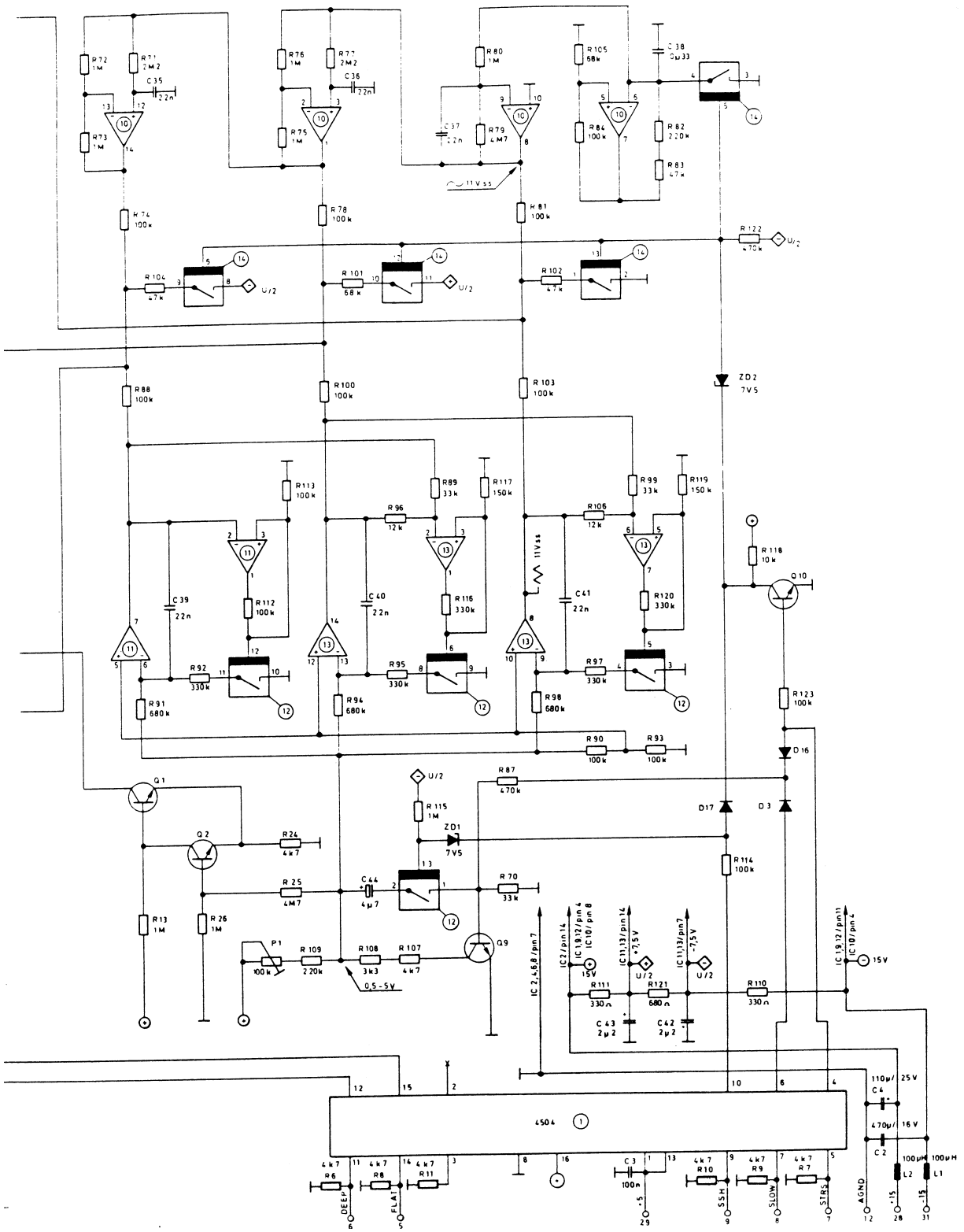
3/ 334



WV 30, Component layout



WV 30, Schematic diagram


R72 1M
R71 2M2
C35 22n
R73 1M
R76 1M
R77 2M2
C36 22n
R75 1M
R80 1M
C37 22n
R79 4M7
11 V s.s.
R105 68k
C38 0µ33
R84 100k
R82 220k
R83 47k
R74 100k
R78 100k
R81 100k
R122 470k
U/2
R104 47k
R101 68k
R102 47k
ZD2 7V5
R88 100k
R100 100k
R103 100k
R113 100k
R89 33k
R117 150k
R96 12k
R99 33k
R119 150k
R106 12k
R118 10k
Q10
C39 22n
R112 100k
C40 22n
R116 330k
11Vss
C41 22n
R120 330k
R92 330k
R95 330k
R97 330k
R91 680k
R94 680k
R98 680k
R123 100k
D16
R90 100k
R93 100k
Q1
R87 470k
D17
D3
R115 1M
ZD1 7V5
Q2
R24 4k7
R114 100k
R25 4M7
C44 4µ7
R70 33k
R13 1M
R26 1M
P1 100k
R109 220k
R108 3k3
R107 4k7
Q9
0,5-5V
IC 2,4,6,8/pin 7
IC2/pin 14
IC 9,12/pin 4
IC10/pin 8
IC11,13/pin 14
+7,5V
IC11,13/pin 7
-7,5V
IC 9,12/pin 11
IC10/pin 4
15V
R111 330Ω
R121 680Ω
R110 330Ω
C43 2µ2
C42 2µ2
4504
110µ/ 25V C4
470µ/ 16V C2
100µH L2
100µH L1
4k7 R6
4k7 R8
4k7 R11
C3 100n
4k7 R10
4k7 R9
4k7 R7
DEEP
FLAT
SSH
SLOW
STRS
AGND
+15
-15
29
9
8
7
12
28
31

11. AF 40 (Audio Board)

The output signal of EF 40 (ORGAN 1, ORGAN 2) is led to the AF 40, controlled in its volume by IC 1, a VCA (voltage-controlled amplifier); the volume level is dependant upon the control voltage at pin 5 or 10. This voltage is adjusted with the swell pedal (05 3), the control current of which (0 to 0.6 mA) is converted into a voltage of 0 to 2 V by two OPAMPs (IC 10).

With P 3 you can adjust the minimal volume level that can be heard with the swell pedal at minimum volume. The LED will be illuminated as soon as the control voltage reaches 2 volts which should be the case when the swell pedal is fully depressed.

The organ signal now adjusted in volume is routed to the reverb summing amp IC 15 (via R B & R 11) to the channel amplifier IC 12 left and right (via R 9 & R 12) and to the multi-channel output (via R 7 & R 10).

The rhythm signal from the drum board DSP 160 uses a similar path; the only difference is that the control signal of the VCA (IC 3) consists of the control voltage VOLRH and a small portion from the swell pedal.

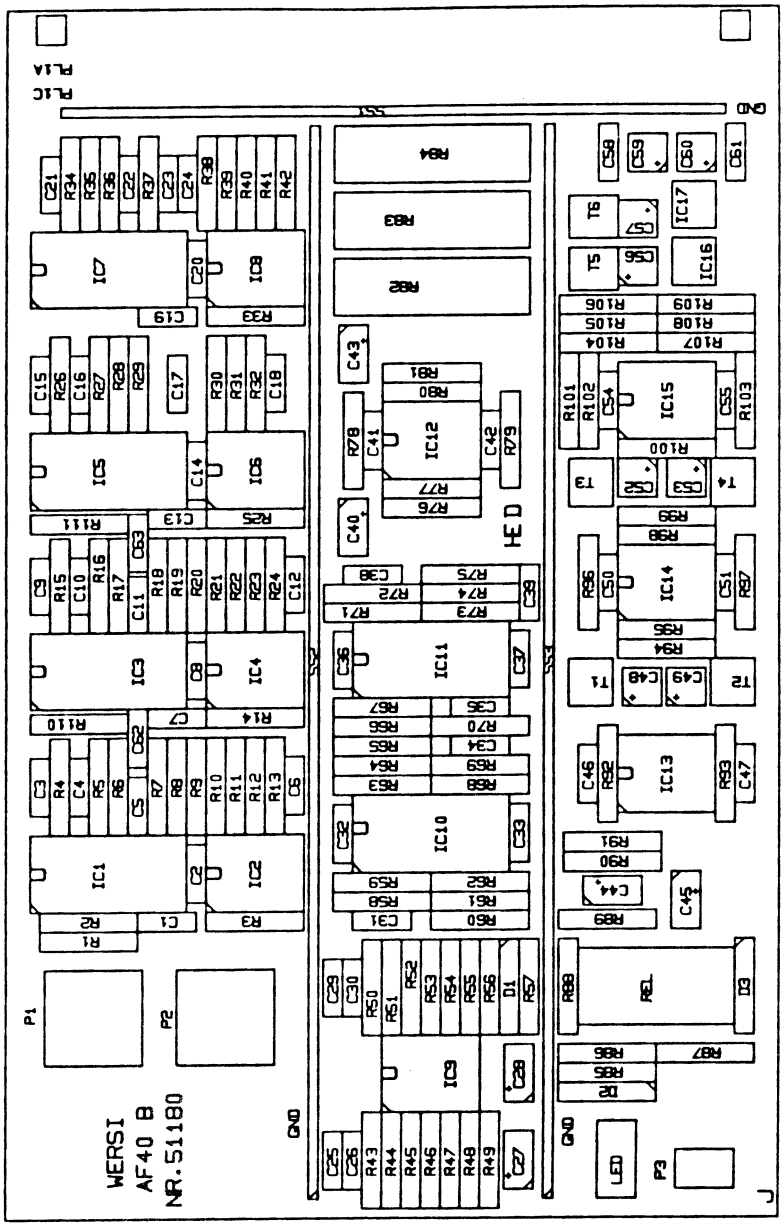
The reverb summing amp leads the organ/rhythm signal to the reverb board DH 11 where the signal is reverberated and - via lines REV 1 and REV 2 - sent back to the AF 40. This signal's amplitude is controlled by IC 7 and added to the original signal via R 39 & R 40.

The organ/rhythm/reverb signal (AF 4/01, AF 4/02) is routed via the main volume control on the connection panel CB 45 (where the overall volume is adjusted) and returns on lines AF 40 Ii and AF 40 12.

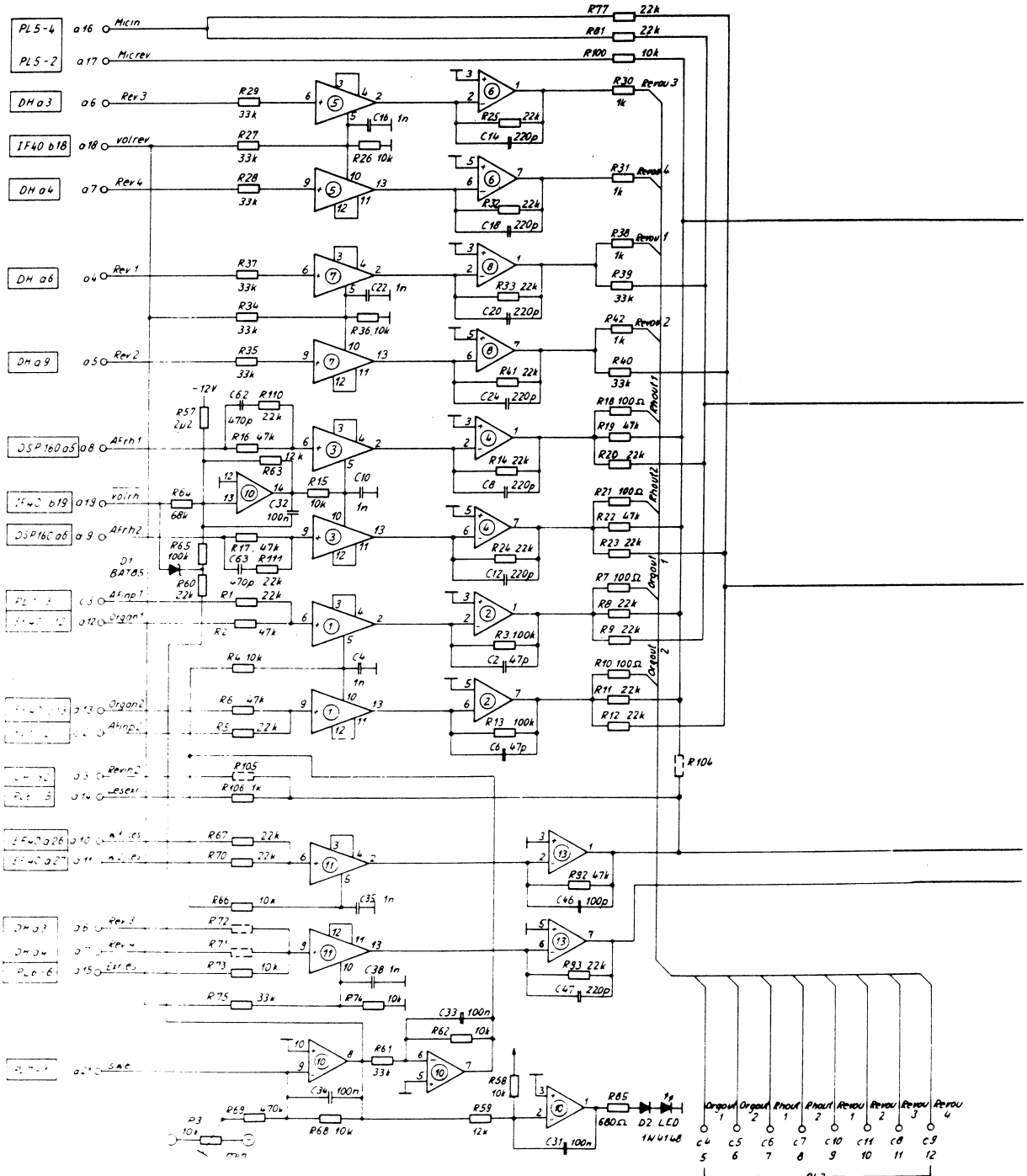
Now the signal is split up; one portion to the headphone amplifier (IC 14, T 1-T4) and one portion to the tone control stage (IC 9, P 1, P2).

The tone control section is followed by a relay with which the audio signal can be switched off.

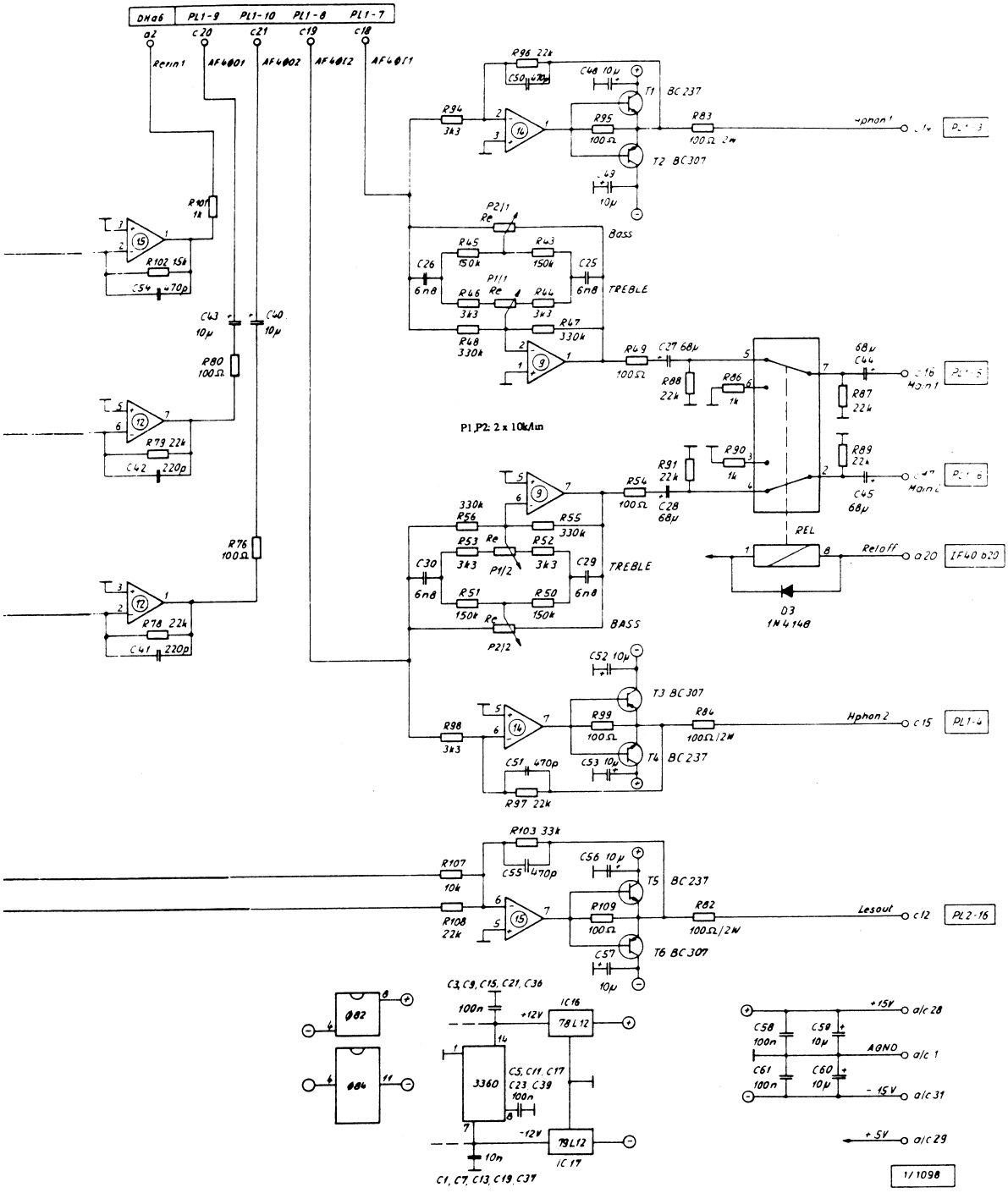
The remaining portion of the circuitry is responsible for the audio supply of the Leslie. One half of the VCA (IC 11) routes the Leslie signal (W 1/LES, W2/LES) to the Leslie amplifier (IC 15, T 5, T 6), depending on the swell pedal position, while the other half adds another reverb signal generated by an external reverb unit.



AF 40, Component layout



AF 40, Schematic diagram


DM06
PL1-9
PL1-10
PL1-8
PL1-7
a2
c20
c21
c19
c18
Rerin1
AF4001
AF4002
AF4012
AF4011
R101 1k
R102 15k
C54 470p
C43 10µ
C40 10µ
R80 100Ω
R79 22k
C42 220p
R76 100Ω
R78 22k
C41 220p
R96 22k
C50 470p
C48 10µ
T1 BC 237
R94 3k3
R95 100Ω
R83 100Ω 2W
T2 BC 307
C49 10µ
Hphon 1
P2/1 Re
Bass
R45 150k
R43 150k
C26 6n8
P1/1
C25 6n8
TREBLE
R46 3k3
Re
R44 3k3
R47 330k
R48 330k
R49 100Ω
C27 68µ
R88 22k
R86 1k
68µ C44
R87 22k
Main 1
P1,P2: 2 x 10k/lin
R90 1k
R91 22k
R89 22k
C45 68µ
Main 2
R54 100Ω
C28 68µ
330k
R56
R55 330k
R53 3k3
Re
R52 3k3
P1/2
C30 6n8
C29 6n8
TREBLE
R51 150k
R50 150k
Re
P2/2
BASS
REL
Reloff
D3
1N4148
C52 10µ
T3 BC 307
R98 3k3
R99 100Ω
R84 100Ω/2W
Hphon 2
C51 470p
C53 10µ
T4 BC 237
R97 22k
R103 33k
R107 10k
C55 470p
C56 10µ
T5 BC 237
R108 22k
R109 100Ω
R82 100Ω/2W
Lesout
C57 10µ
T6 BC 307
C3, C9, C15, C21, C36
100n
IC16
+12V
78L12
3360
C5, C11, C17
C23, C39
100n
-12V
78L12
IC17
10n
C1, C7, C13, C19, C37
Ø82
Ø84
C58 100n
C59 10µ
C61 100n
C60 10µ
+15V
AGND
-15V
+5V
1/1098

B. Control Panels

1. KD 11 (Manual Board)

The dynamic measurement is based on the principle of time measurement. For this purpose, each key is connected to a switch. The time from the opening of the rest contact to the closing of the working contact is measured. 8 switches are combined in 1 matrix address. For 5 octaves (61 keys), 8 matrix addresses are needed. These matrix addresses are grounded one after the other, and the state at the 16 contacts is polled. The rate at which this polling occurs can be adjusted via the coding switch, whose position is checked only after resetting, however. If this time is very short, the key must be depressed very quickly for the loudest value to be reached.

The data is transmitted to a 2 byte parallel port. The first port (IC 5) contains the pitch and whether the sound is to be switched on or off; the second contains the dynamic value. When the dynamic value is recorded, a flip-flop (IC 8) is set which triggers a FIRO at the master. When reading the port, only the key (IC 5) is read which has the FIRO in its upper bit (via IC 4, pin 13). Thus, it can be determined whether it has actually been this manual that triggered the FIRQ request.

If this is true, the dynamic value can be read while the FIRQ flip4lop is reset simultaneously.

Furthermore, the interrupt can be blocked with the second flip-flop of IC 8. IC 7 provides the address decoding process.

The remaining part of the board serves for pedalboard matrix-interrogation and for jumper-interrogation (Ju 7-14).

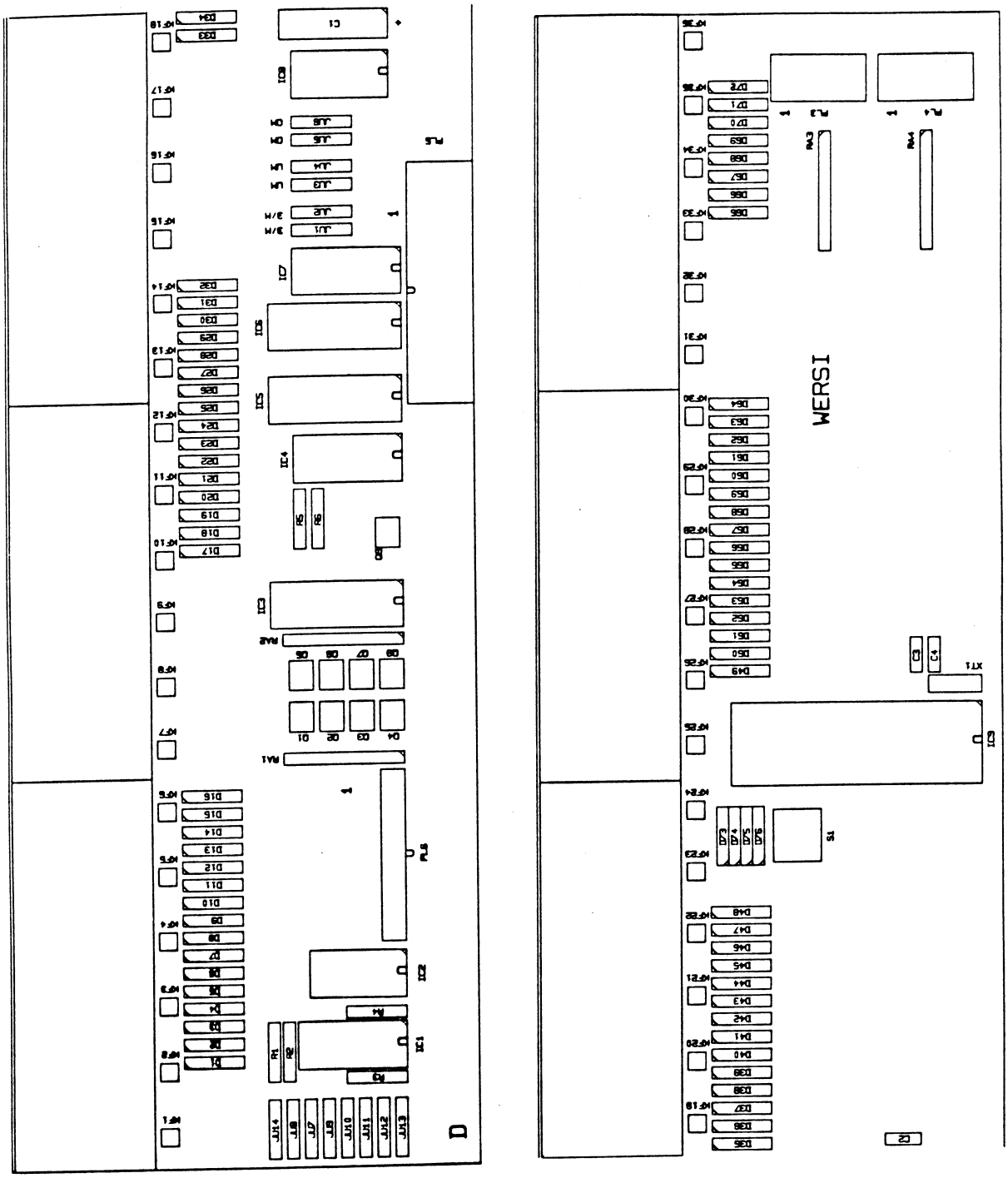
2. KD 2IKD 4 (Manual Extension Boards)

These boards serve as extension boards for the KD 11 to reach the required length of 4 or 5 octaves.

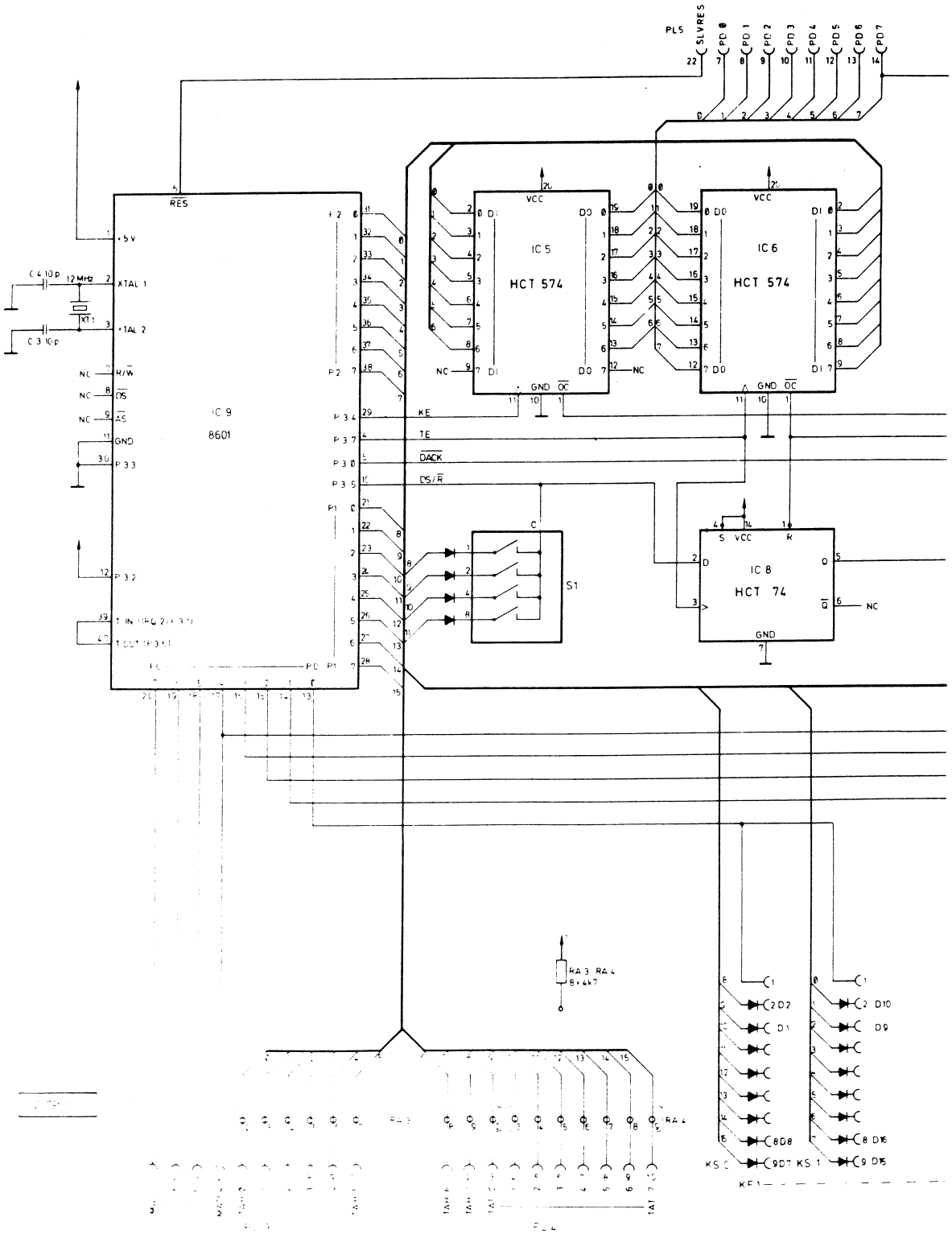
3. Pedalboard

The pedalboard is connected to the KD 11 via Plug 6 and also use the matrix method for keying. Each pedal will always connect one PE.. line with a SEL. - line. The pedalboard matrix diagram shows the combination used by each

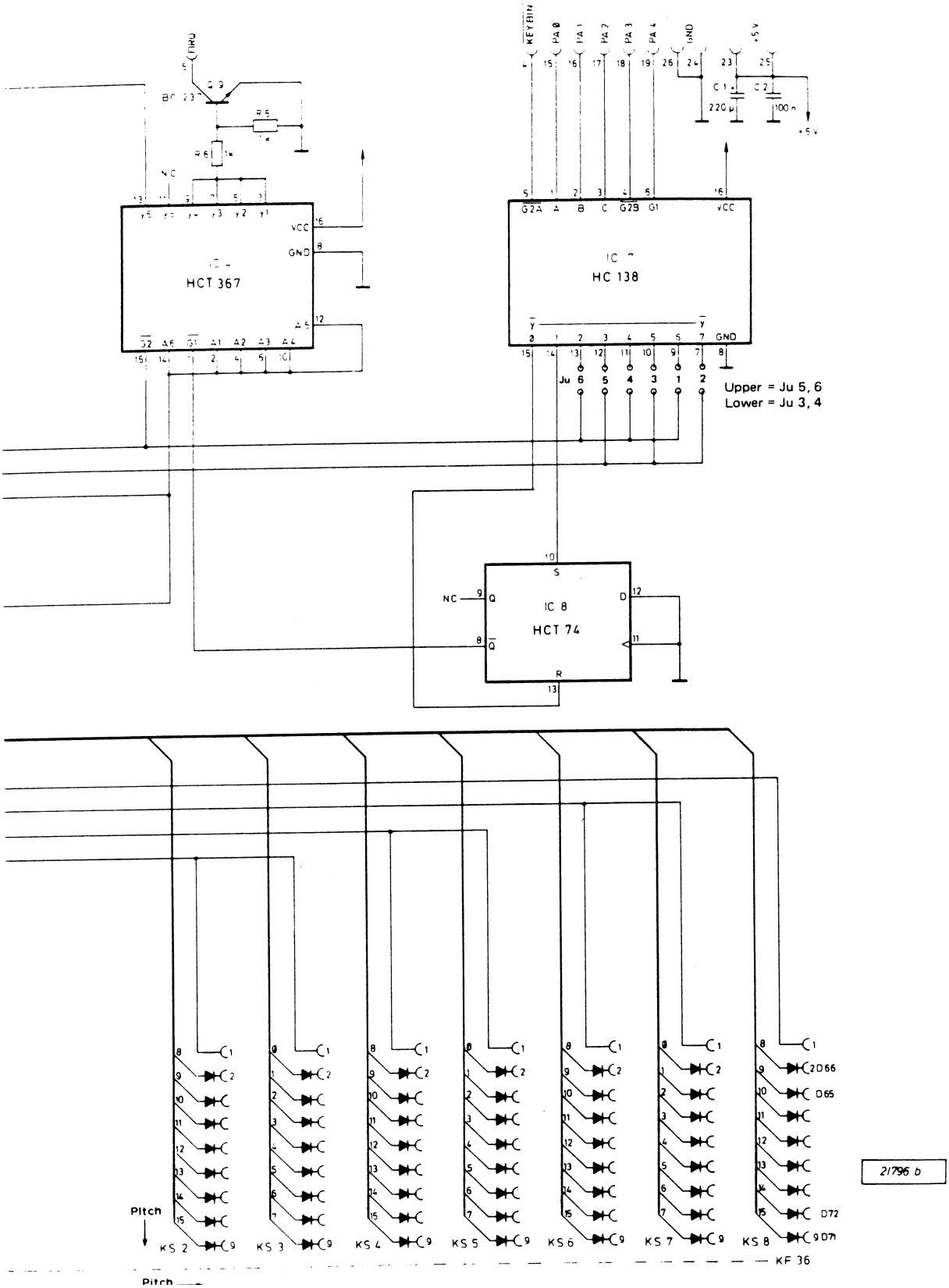
pedal.

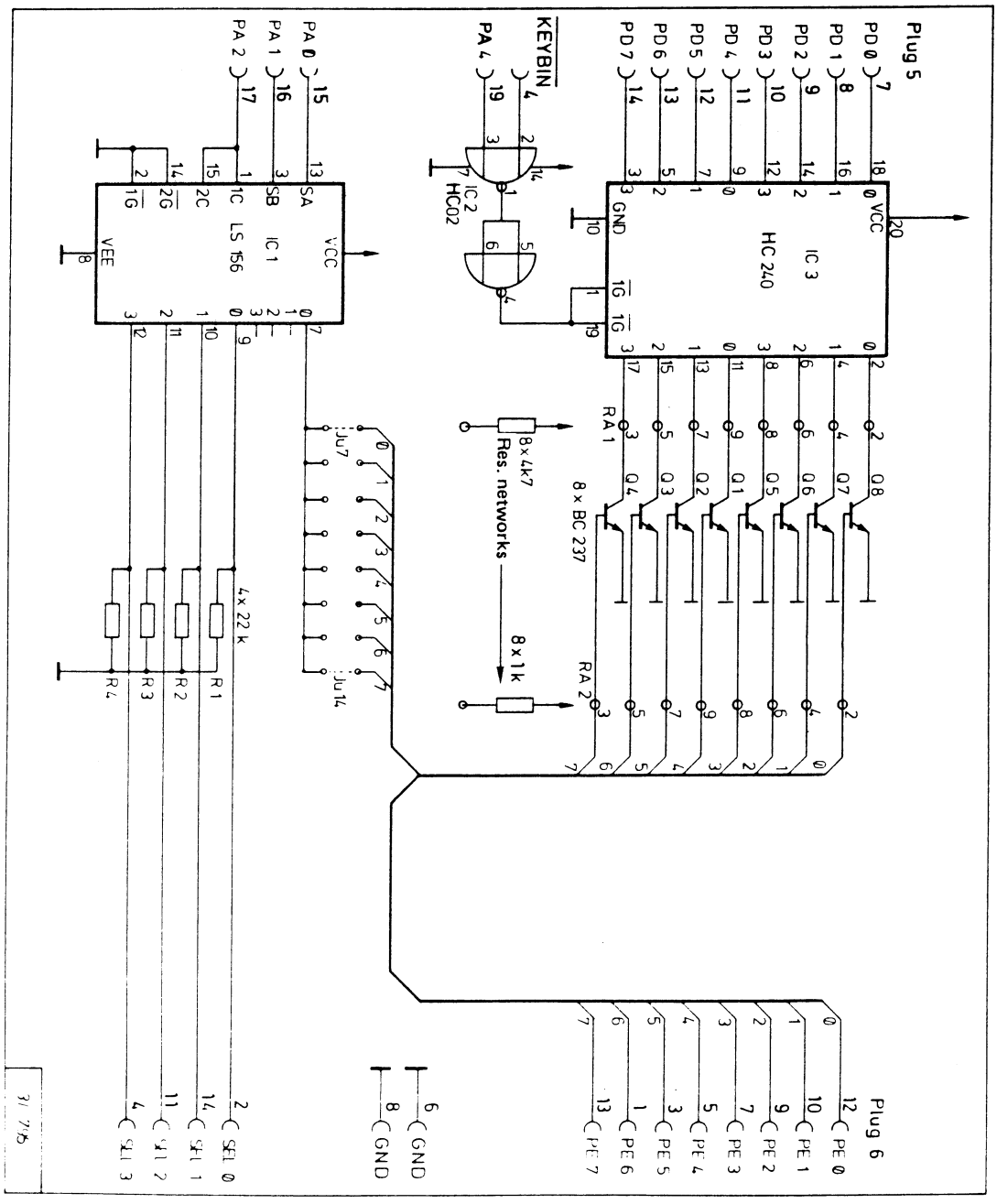


KD 11, Component layout

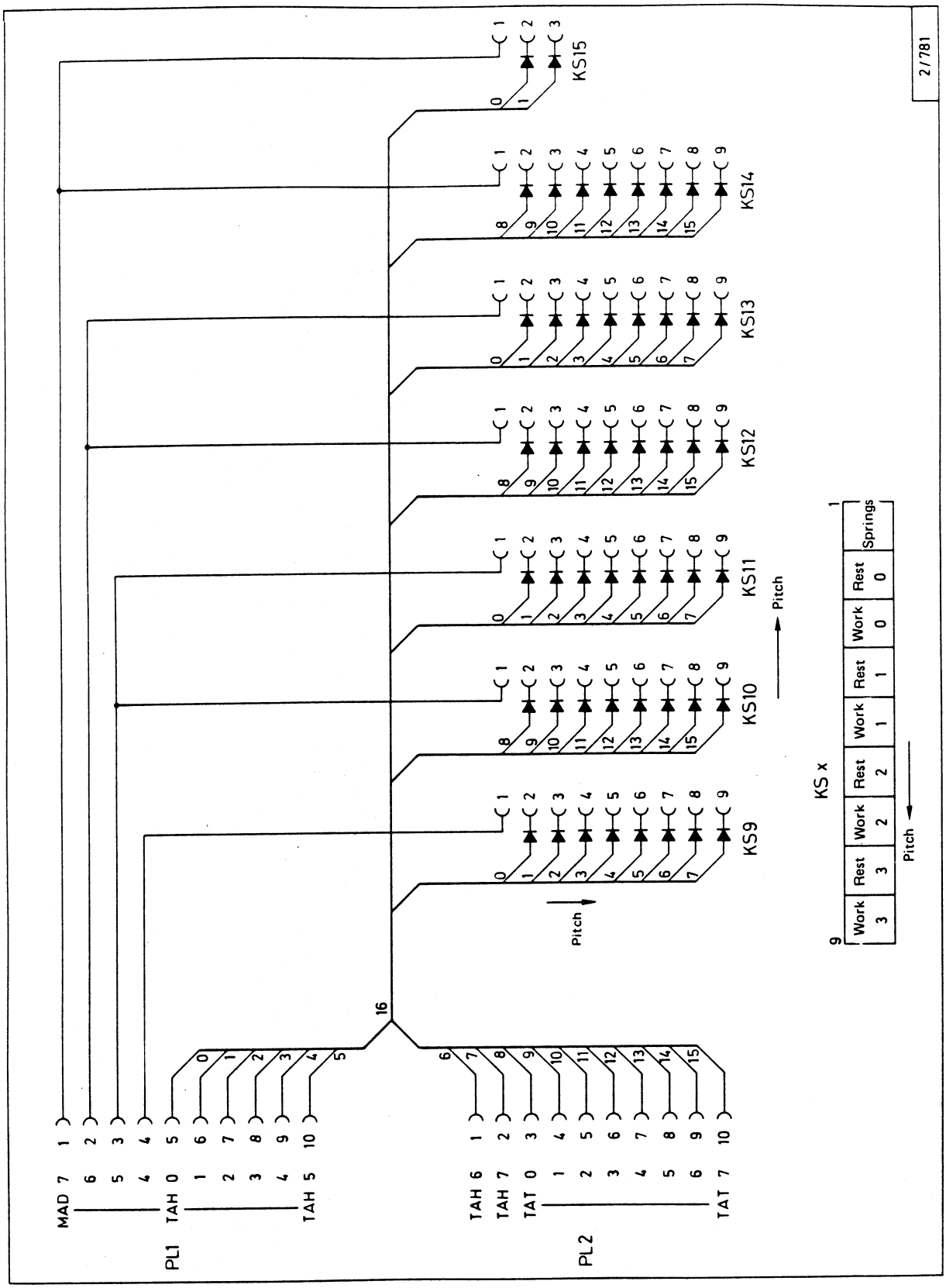


KD 11/a, **Schematic diagram**

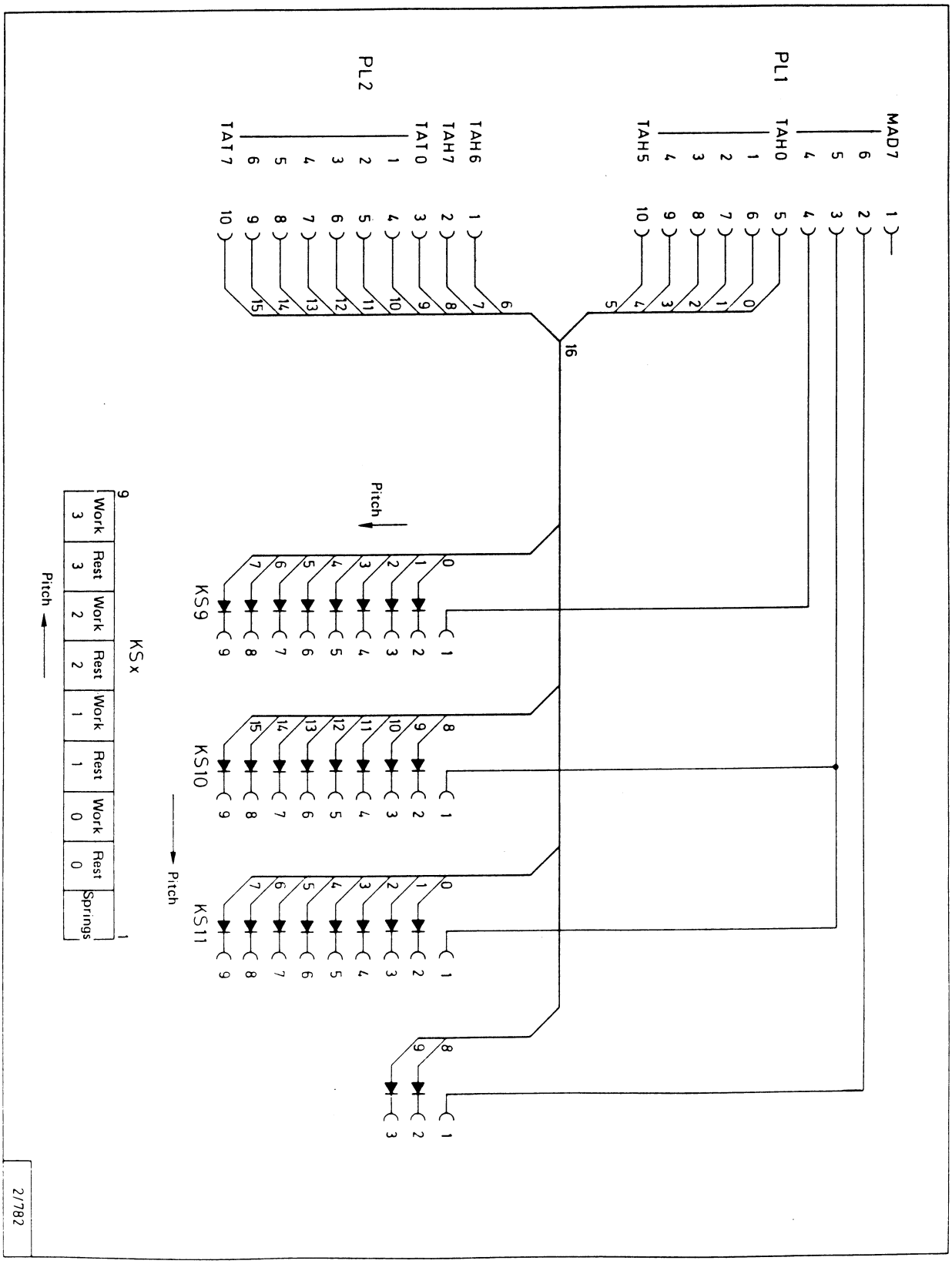

IRQ
Q 9
BC 237
R 5
R 6
N C
HCT 367
VCC
GND
KEYBIN
PA 0
PA 1
PA 2
PA 3
PA 4
GND
+5 V
C 1
220 µ
C 2
100 n
+5 V
HC 138
G2A
A
B
C
G2B
G1
VCC
GND
Ju 6 5 4 3 1 2
Upper = Ju 5, 6
Lower = Ju 3, 4
IC 8
HCT 74
NC
S
Q
D
R
Pitch
KS 2
KS 3
KS 4
KS 5
KS 6
KS 7
KS 8
D66
D65
D72
D71
KF 36
21796 b



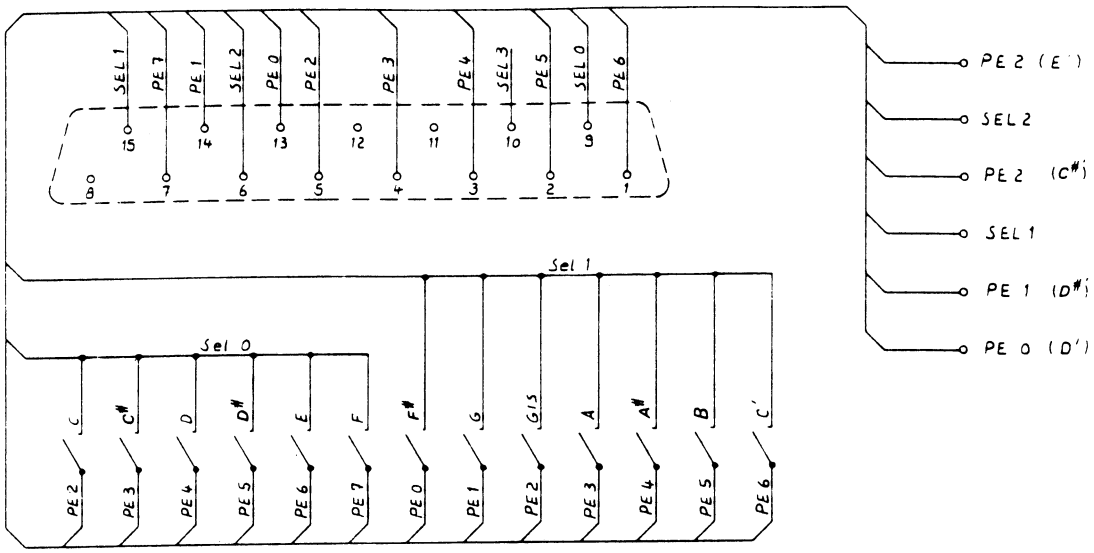
KD 11/b, Schematic diagram



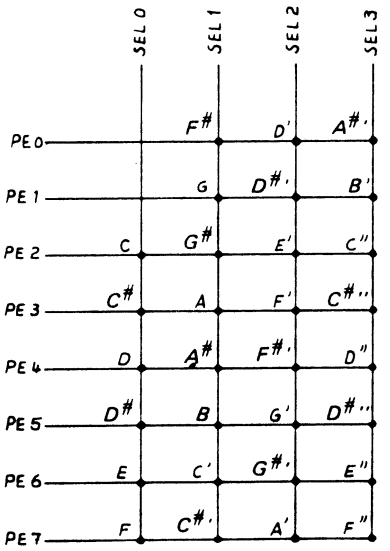
KD 2, Schematic diagram



KD 4. Schematic diagram



PK 40, Schematic diagram



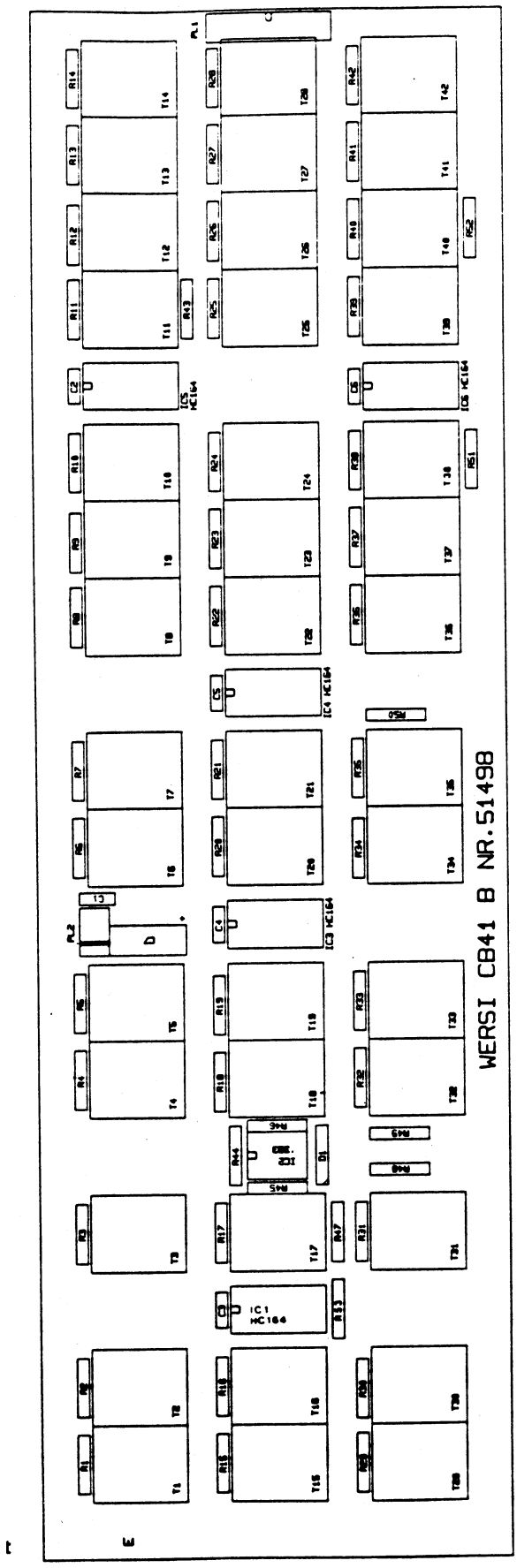
Pedalboard matrix

4. CB 41, CB 42, CB 43 (Main Control Panels Left, Center, Right)

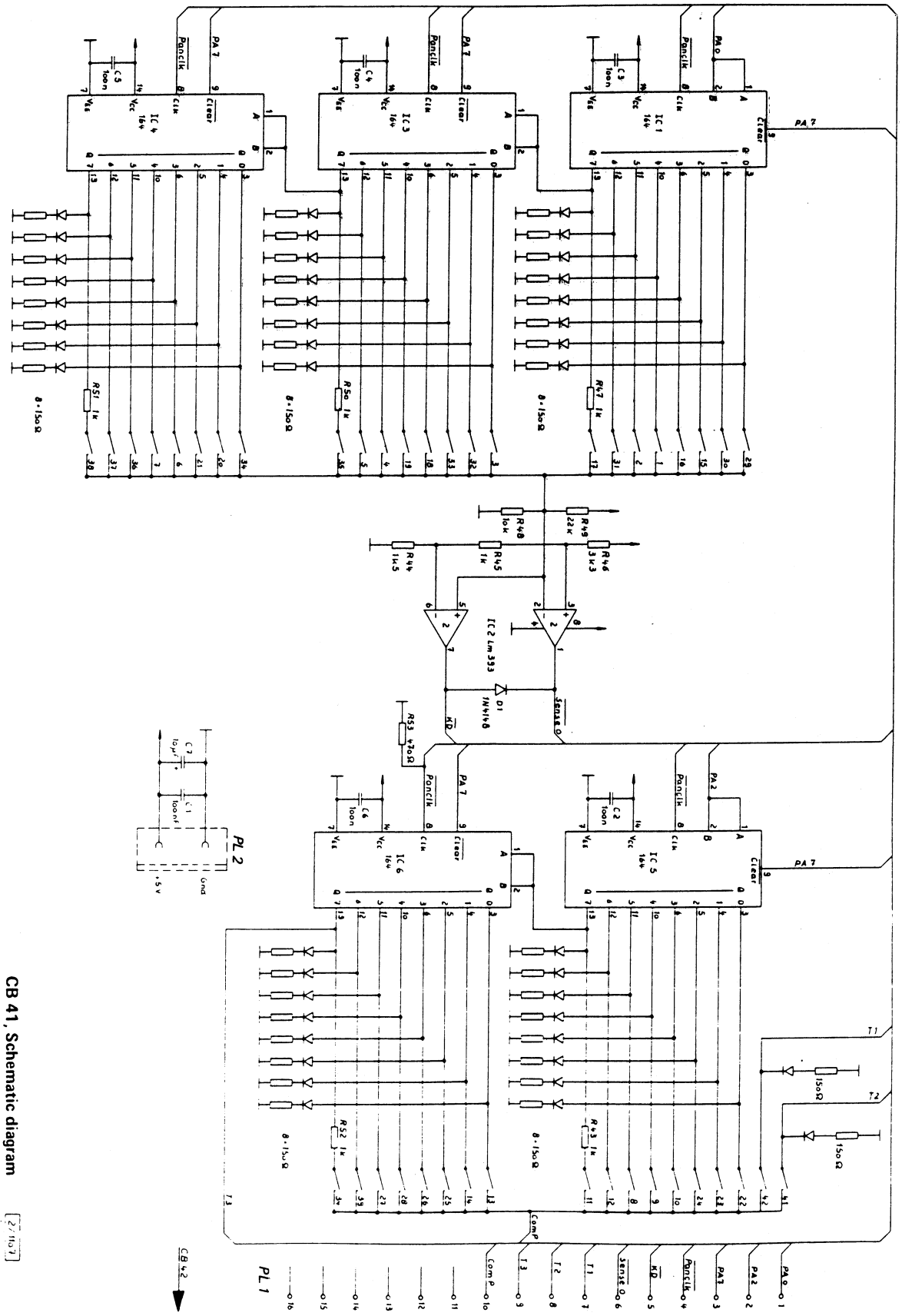
These boards carry the switch recognition and the activaing of the LEDs. Furthermore, the CB 42 carries the LCD display plus outputting IC 1 (HC 174). And on the CB 43 there is the on/off switch with integrated bi-color LED.

The switches (and their appropriate LEDs) are arranged in 5 groups with 24 switches each. If no switch is depressed, both the SENSE and the KD output of the respective pair of comparators are set to +5 V.

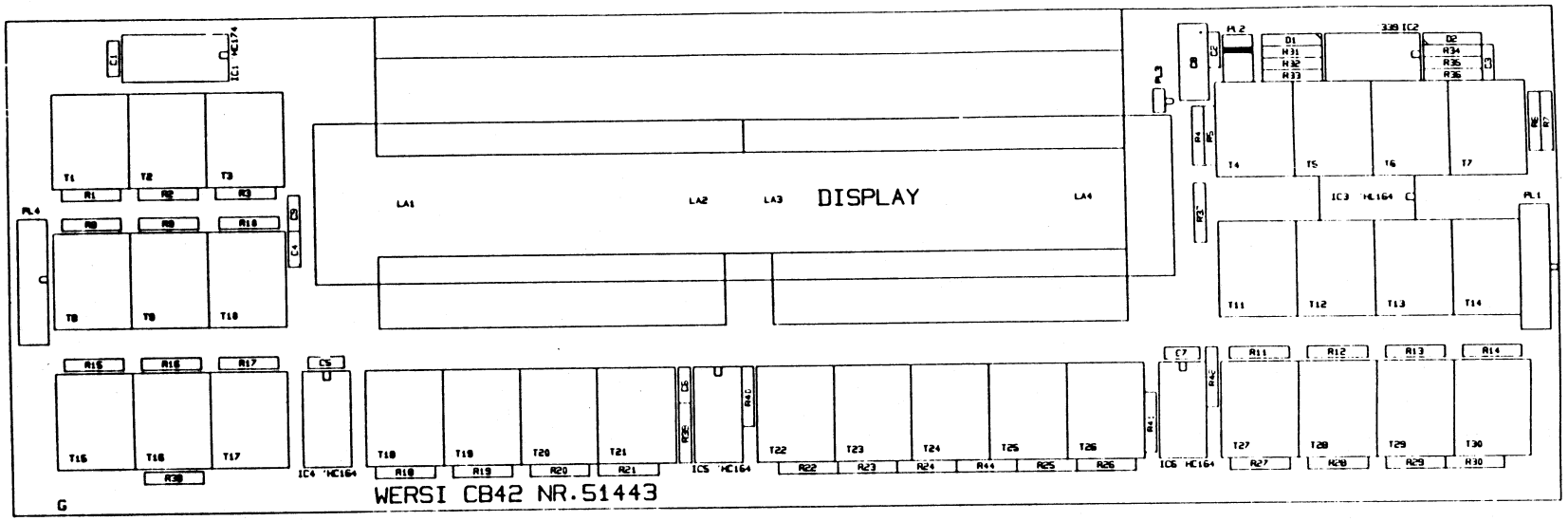
A momentary switch closure results in a Sense and KD pulse, which is applied to the CPU's data bus. This sense pulse occupies a specific time slot in the CPU's sequence program and instructs the CPU to initiate the function for that time slot. The CPU, in turn, sends a serial data code to the appropriate shift register (74 HCT 164), designating the LEDs to light up.



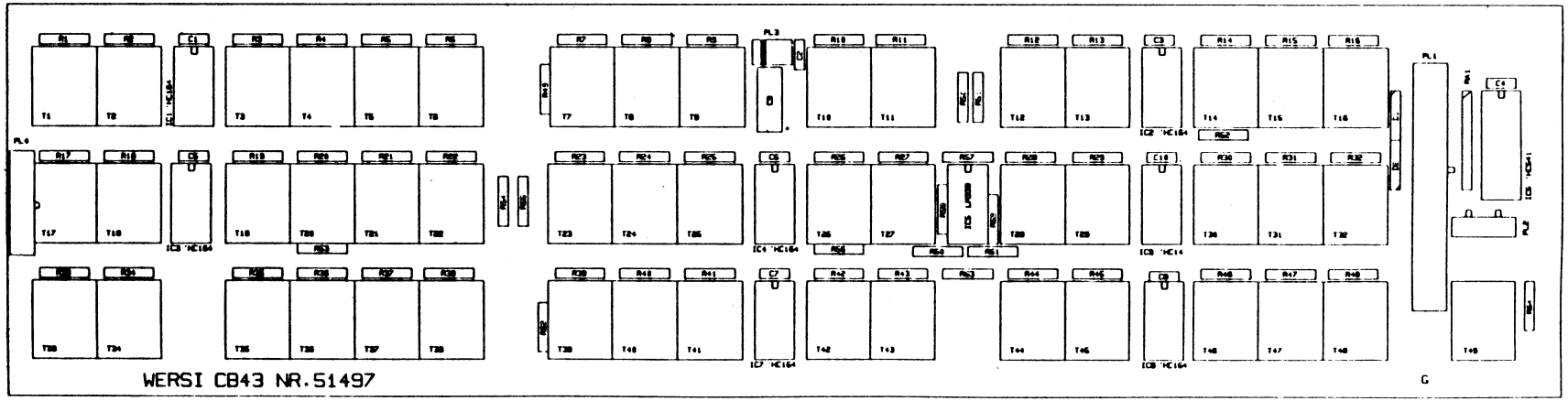
CB 41, Component layout



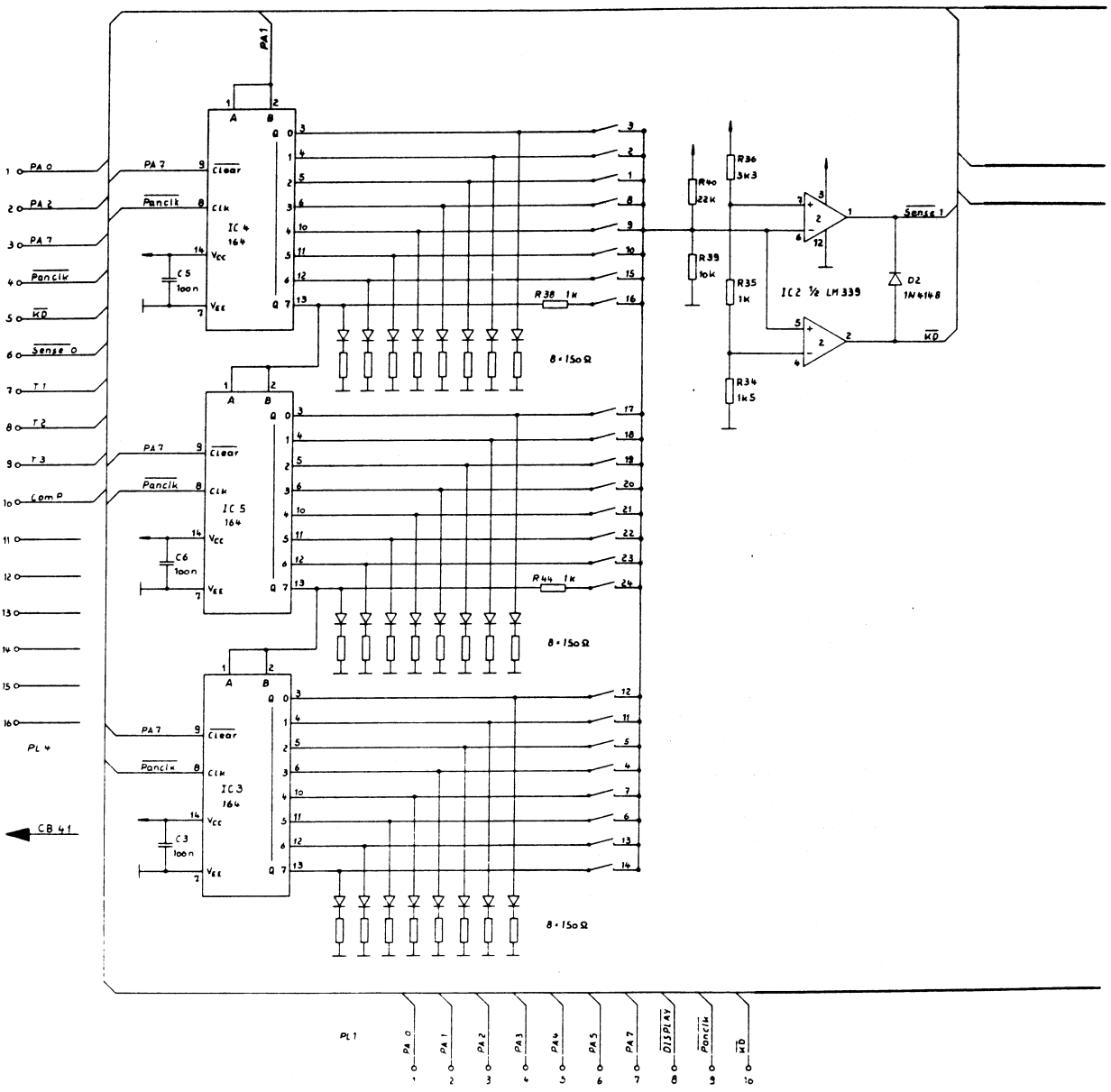
CB 41, Schematic diagram [2/1107]



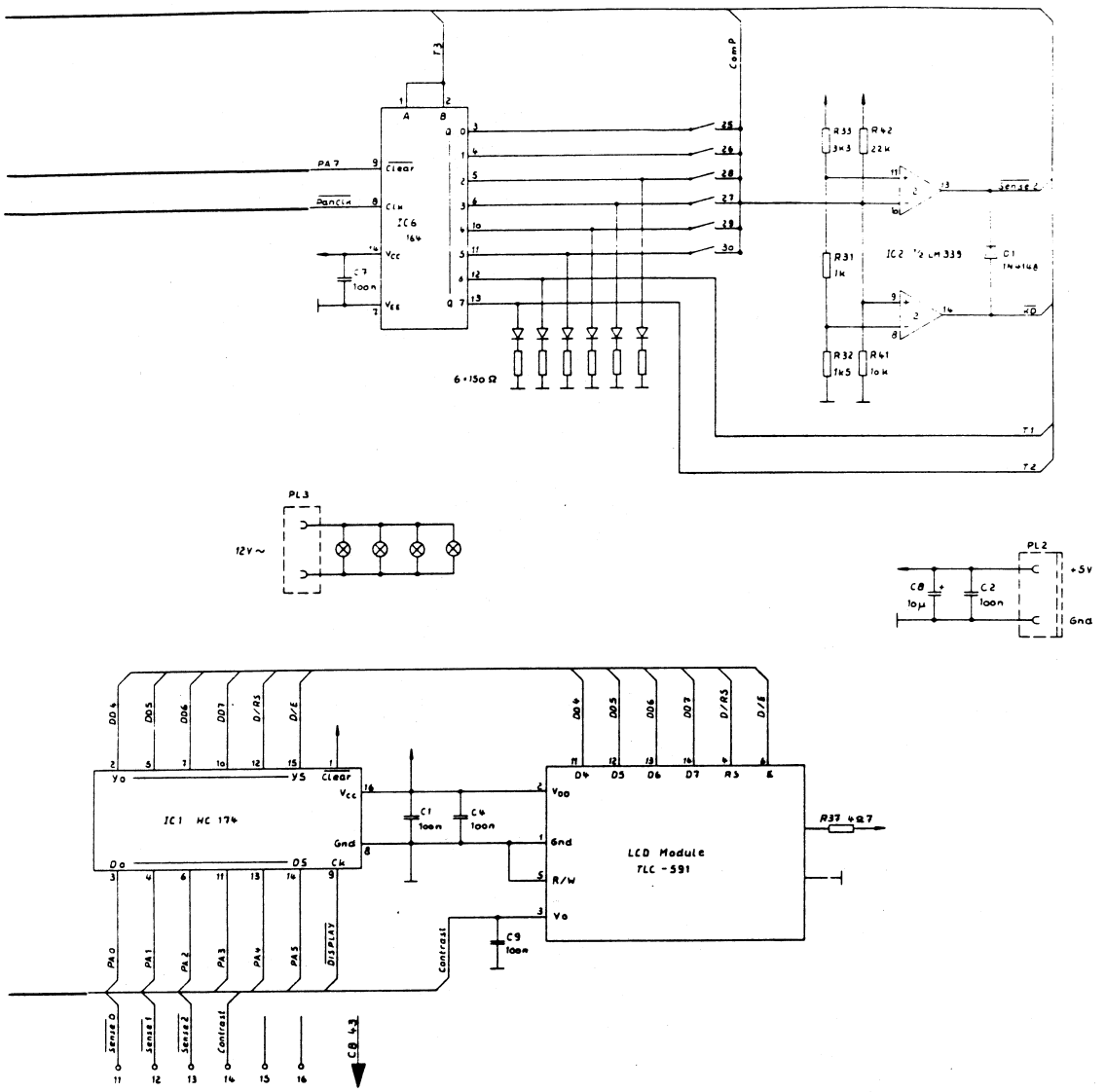
CB 42, Component layout



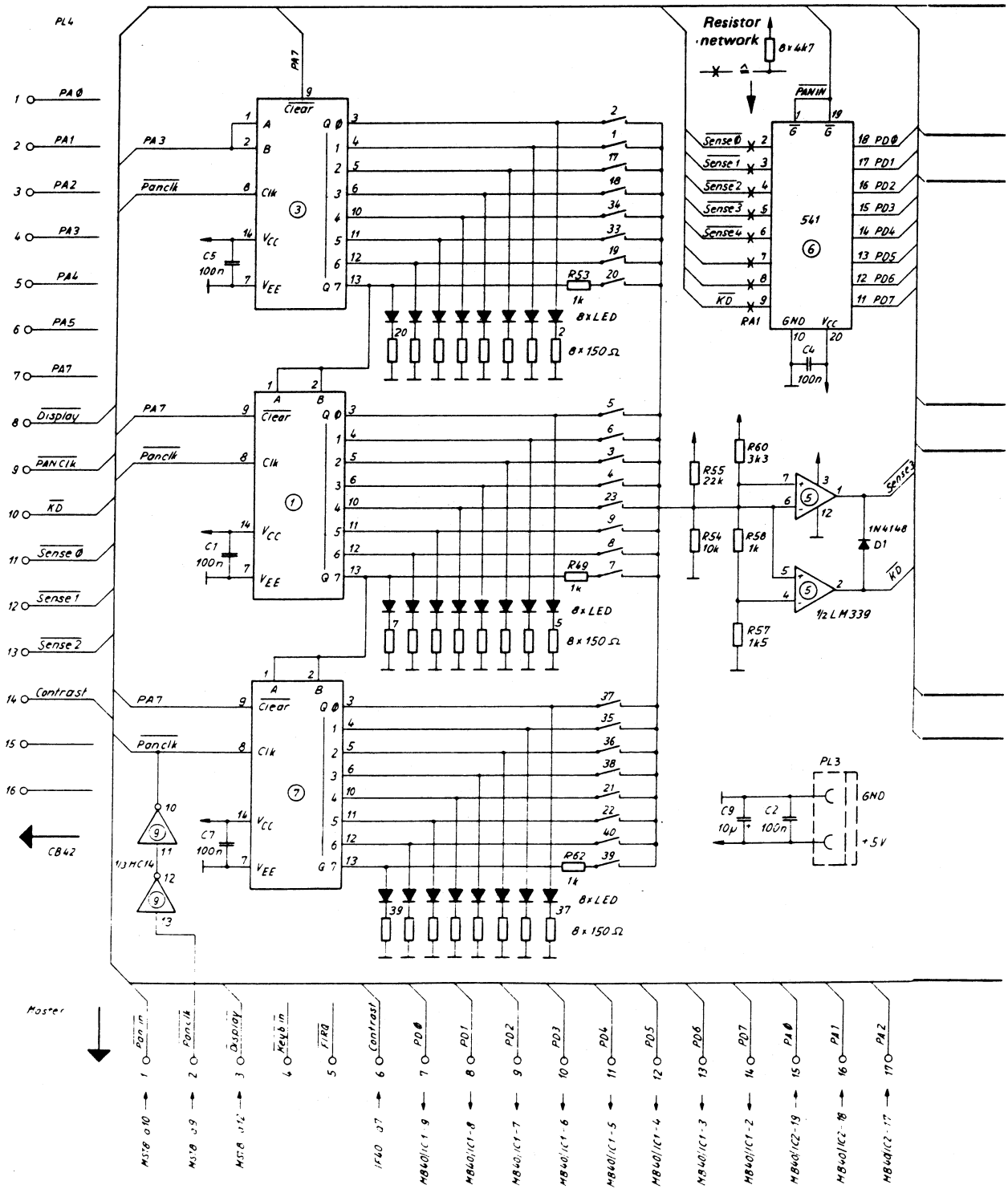
CB 43, Component layout



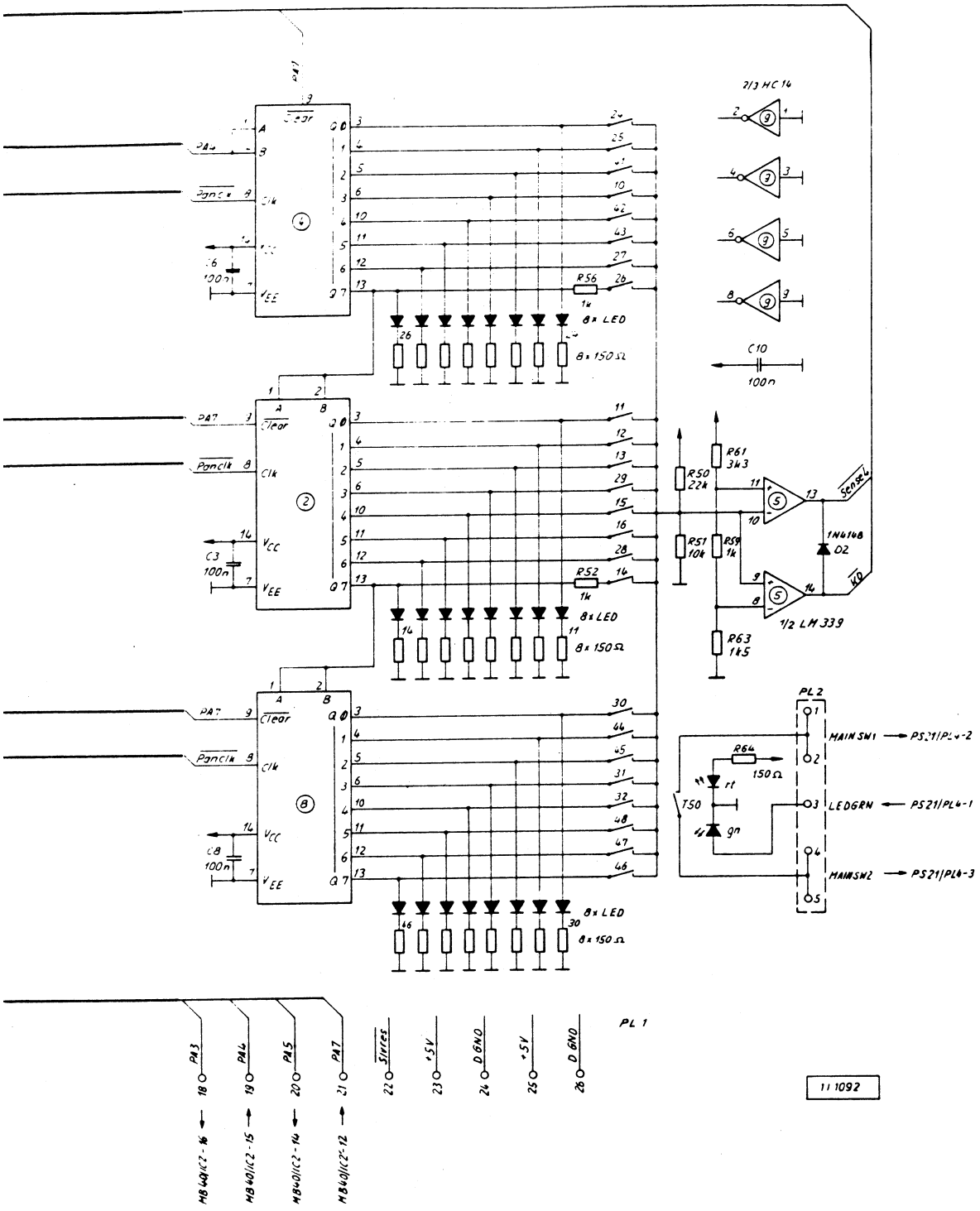
CB 42, Schematic diagram


IC6
164
IC2 1/2 LM 339
R33
3k3
R42
22k
R31
1k
R32
1k5
R41
10k
C1
1N4148
C7
100n
6 x 150 Ω
PA7
Clear
Clock
Vcc
VEE
Comp
T1
T2
PL3
12V ~
PL2
+5V
Gnd
C8
10µ
C2
100n
IC1 HC 174
Clear
Vcc
Gnd
C1
100n
C4
100n
LCD Module
TLC - 591
R/W
Vo
Voo
R37 4Ω7
C9
100n
Contrast
DISPLAY
Sense0
Sense1
Sense2
C8 43

1/ 11o9

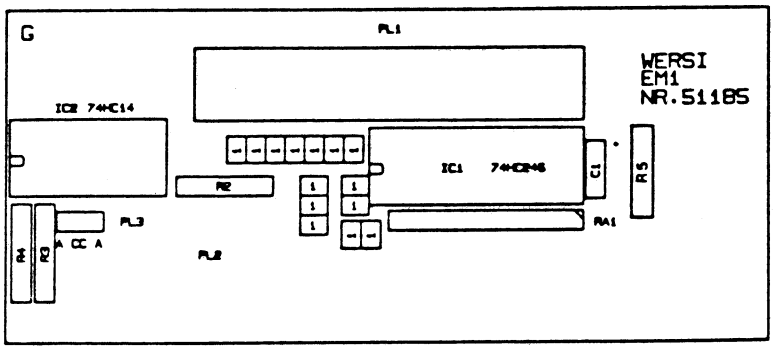


CB 43, Schematic diagram

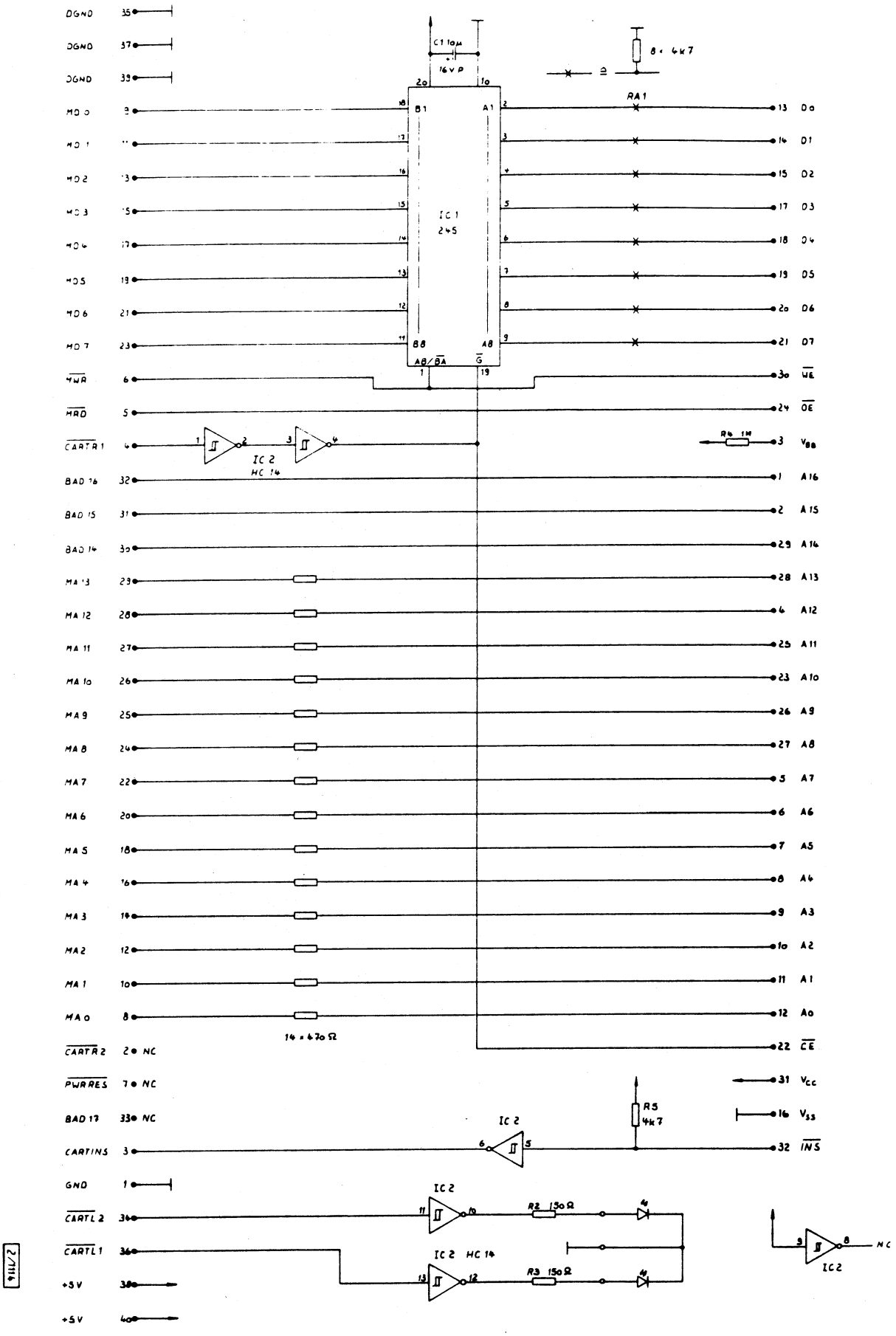

PA7
Clear
Pgmclk
Clk
VCC
VEE
C6 100n
C3 100n
C8 100n
8 x LED
8 x 150Ω
RS6 1k
RS2 1k
1/3 HC 14
C10 100n
R61 3k3
R50 22k
R51 10k
R59 1k
R63 1k5
1N4148 D2
1/2 LM 339
Sense
PL2
MAIN SW1
MAIN SW2
R64 150Ω
TSO
rt
gn
LEDGRN
PS21/PL4-1
PS21/PL4-2
PS21/PL4-3
PL 1
PA3
PA4
PA5
PA7
Sirres
+5V
D GND
11 1092

5. **EM 1 (External Memory)**

This board is the interface to the external memory card. The data bus driver (IC 1, HC245) feeds through the data of the Mem.Card to the master data bus as soon as access to them is required.



EM 1, Component layout



EM 1, Schematic diagram

AM 320-01-808

6. CB 40 (Potentiometer Board)

Basically, this board is a 40-channel multiplexer which feeds through the voltages adjusted with the volume control potentiometers to the output IC 8. Selection is done by means of the potentiometer address, which the co-master writes in IC 1 (HC 174).

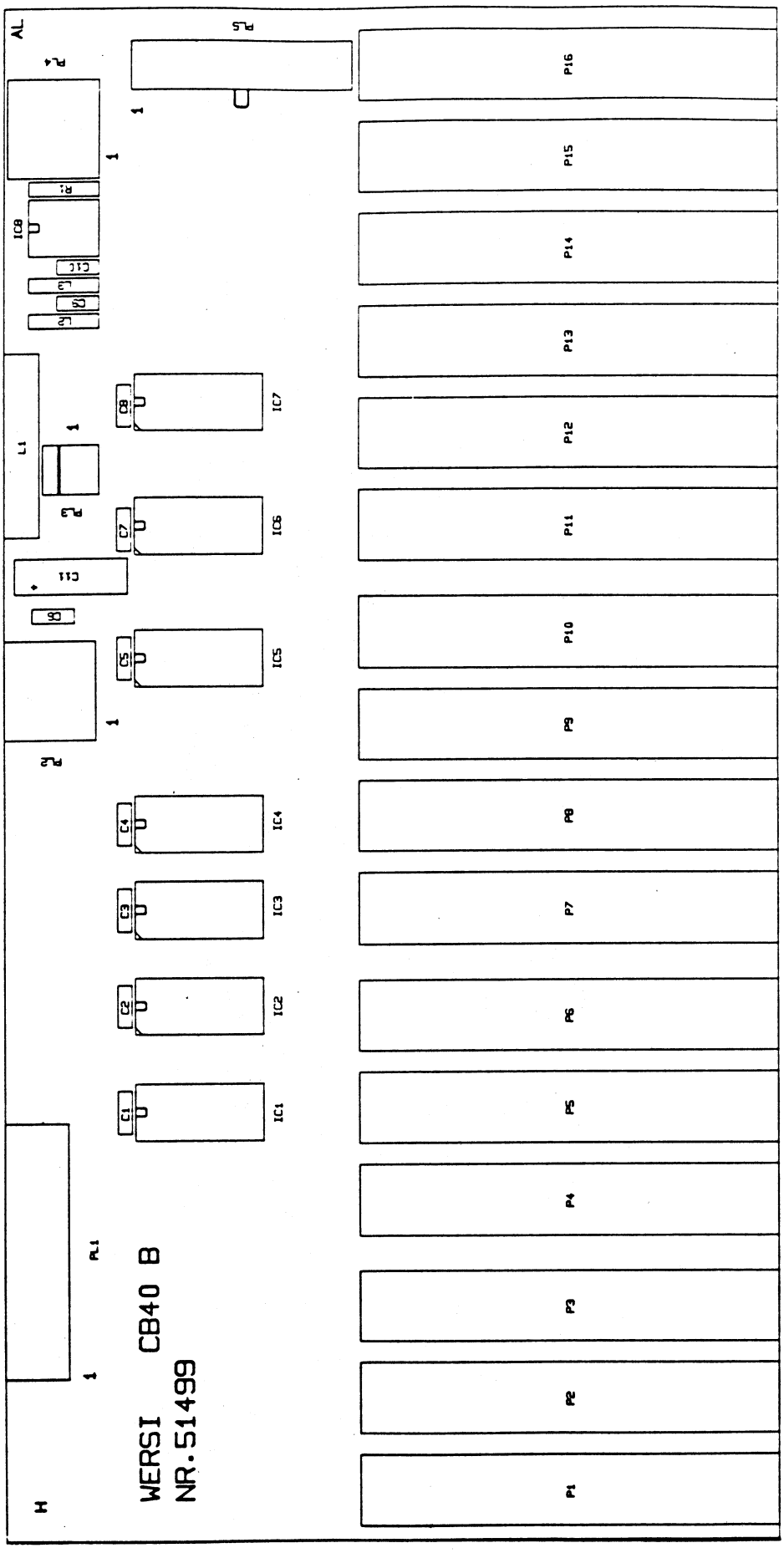
The multiplexed analog output of IC 8 goes to an Analog-to-Digital Converter located on the CO 1 board.

7. CB 48 (VCF, Touch, Glide)

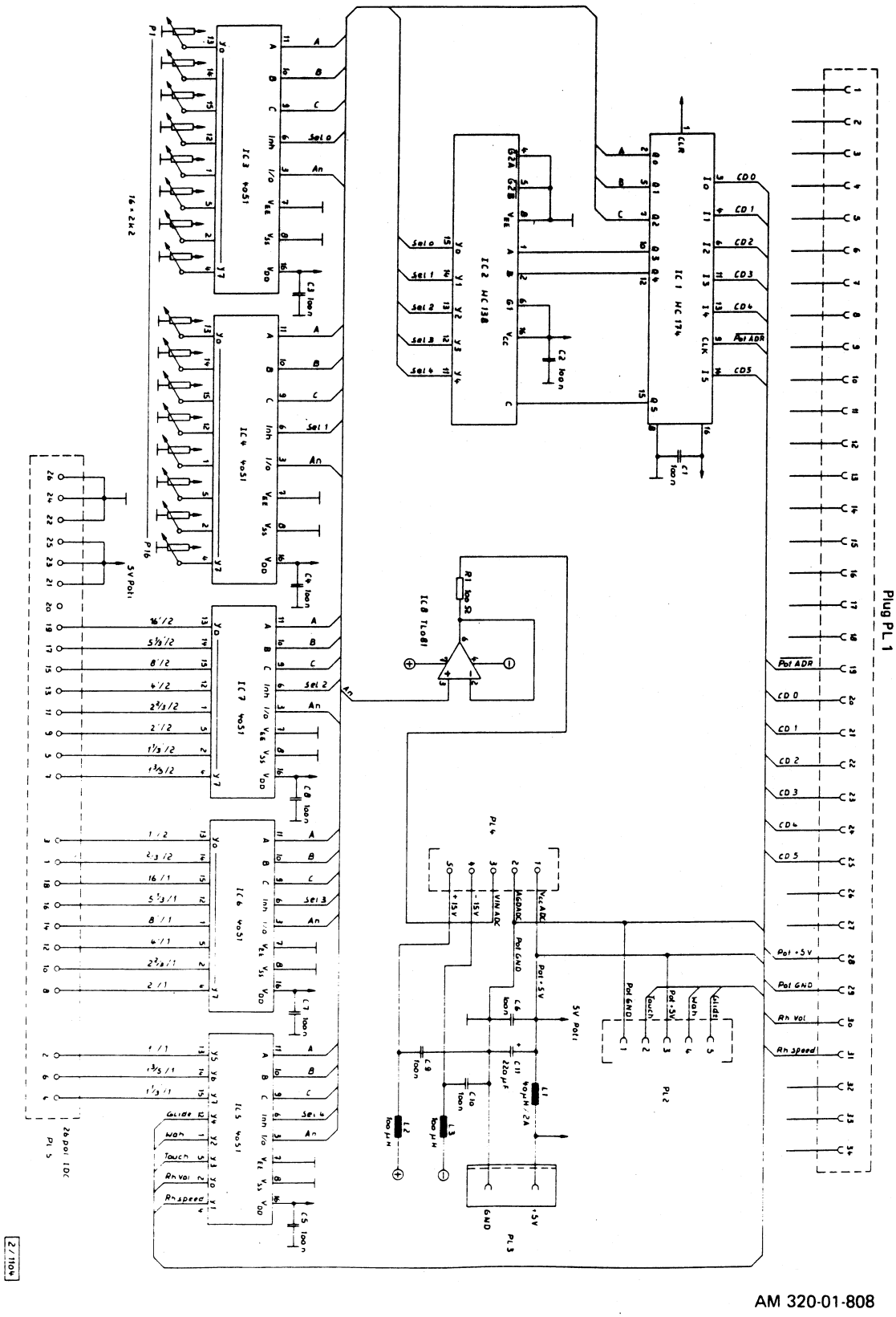
On this board the signal of the two touch sensors is processed (IC 1) and converted into a voltage between 0 and 4 V. And with the two potentiometers the voltages for VCF and Glide are produced.

8. DR 409, DR 410 (Drawbar Board)

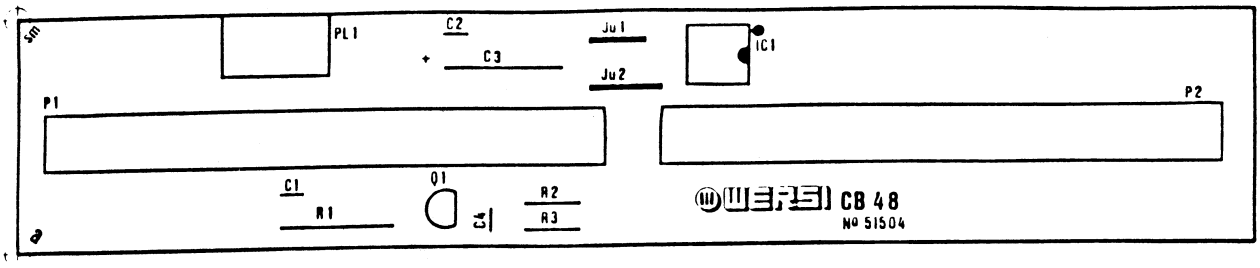
The drawbar potentiometers are located on these boards. They are connected to CB 40.



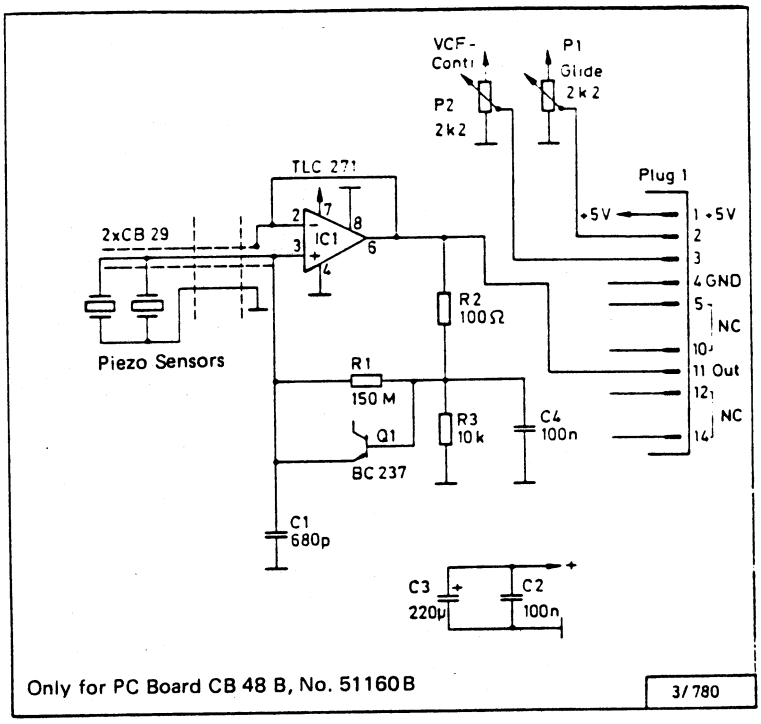
CB 40, Component layout



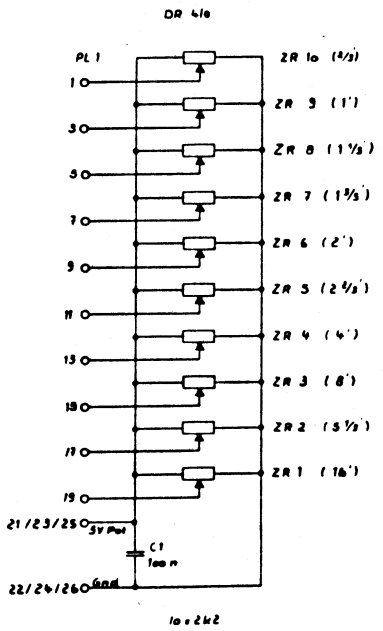
CB 40, Schematic diagram

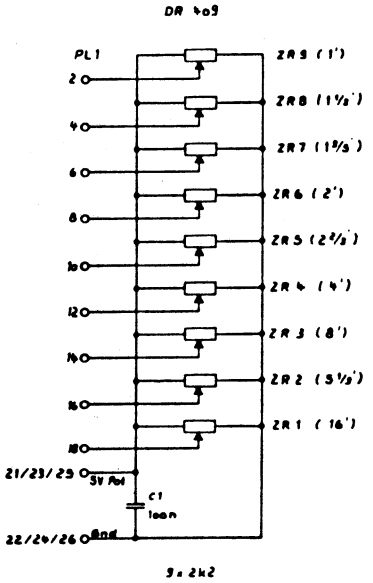


CB 48, Component layout



CB 48, Schematic diagram





DR 410, Schematic diagram

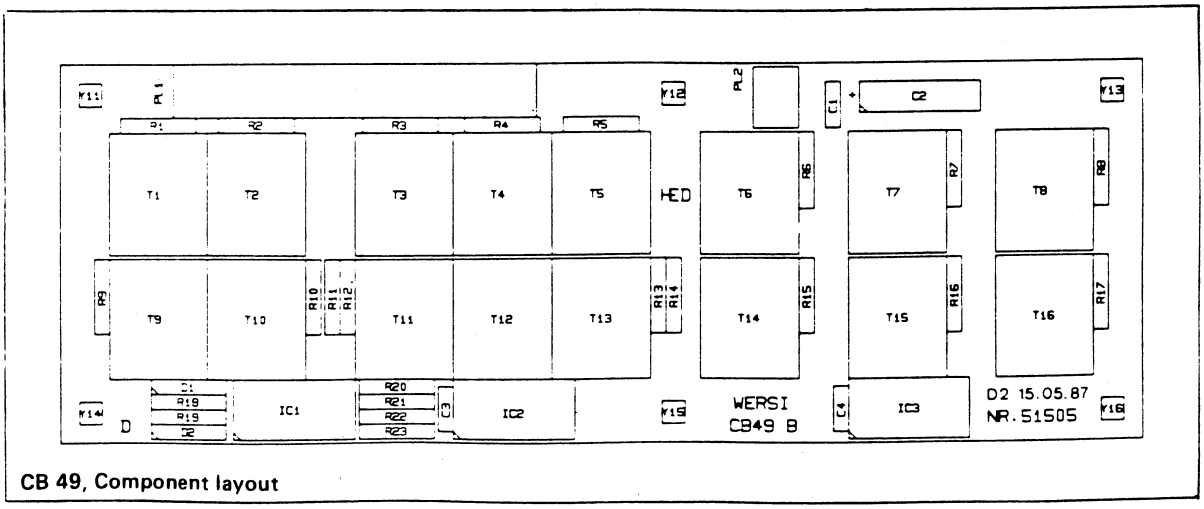
DR 409, Schematic diagram

9. CB 44, CB 49 (Rhythm Control Panels)

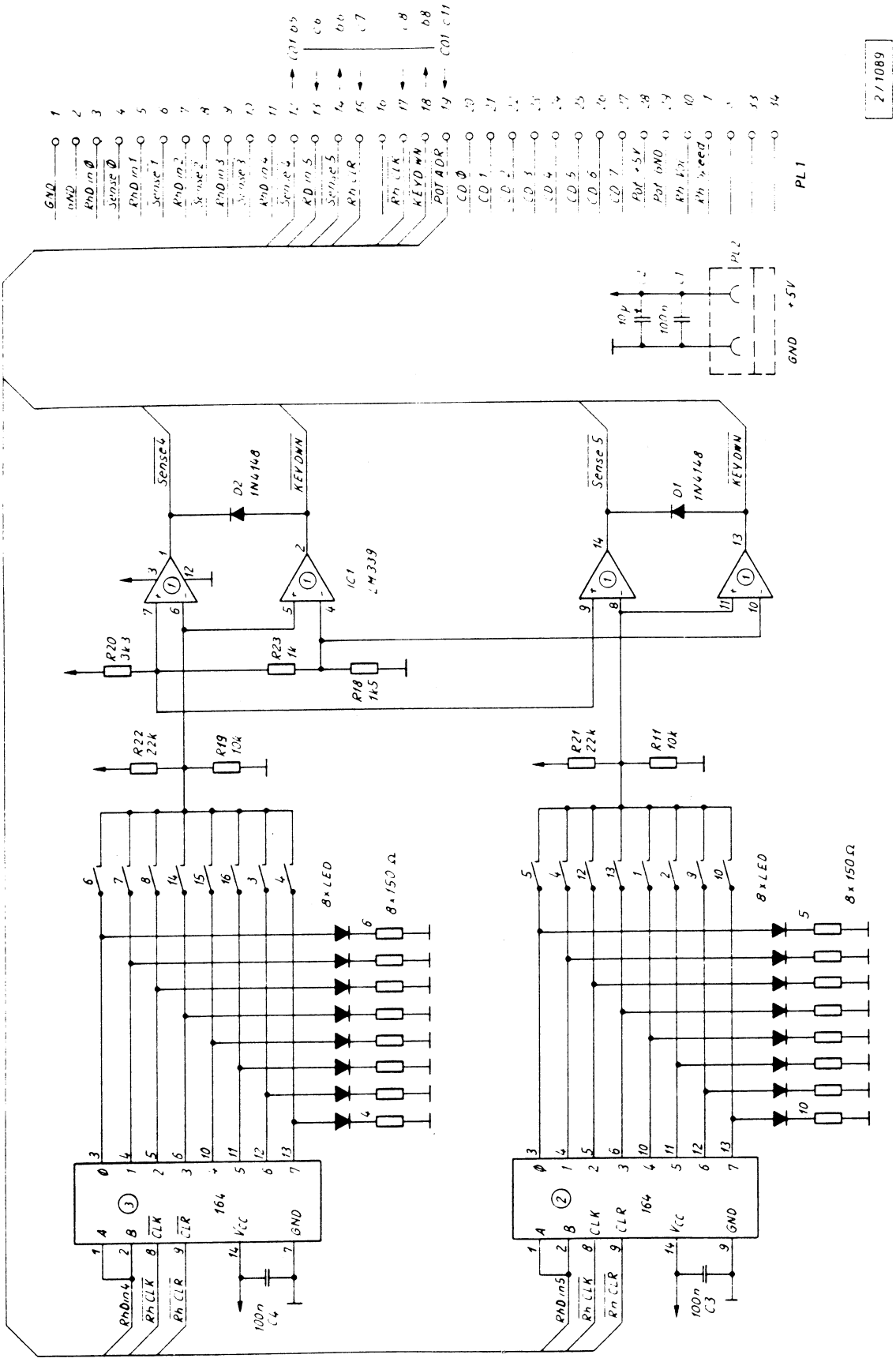
These rhythm control panels have the same functions as the boards CB 41... CB 43. However, they are connected to CO

1.

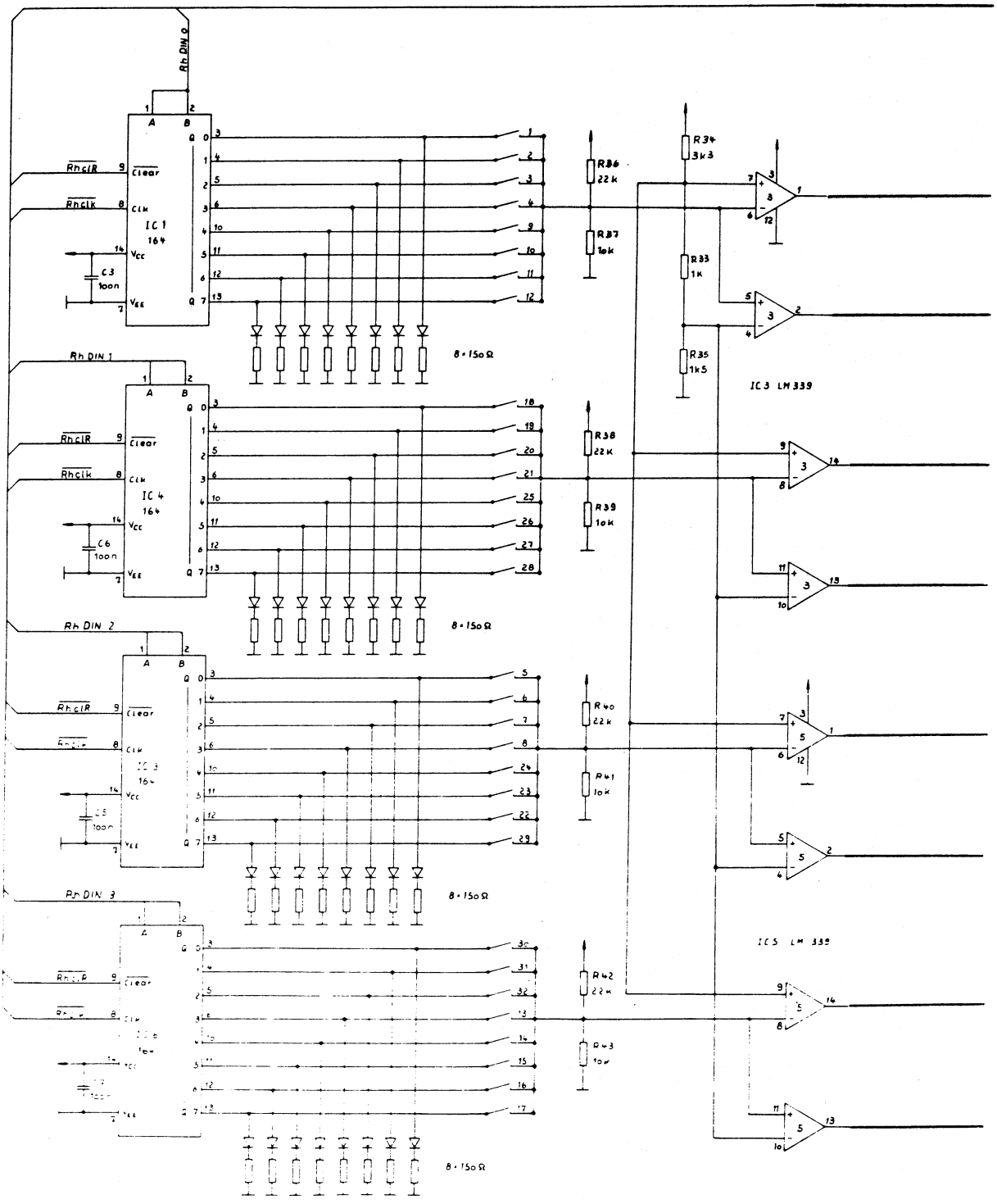
CB 44, Component layout



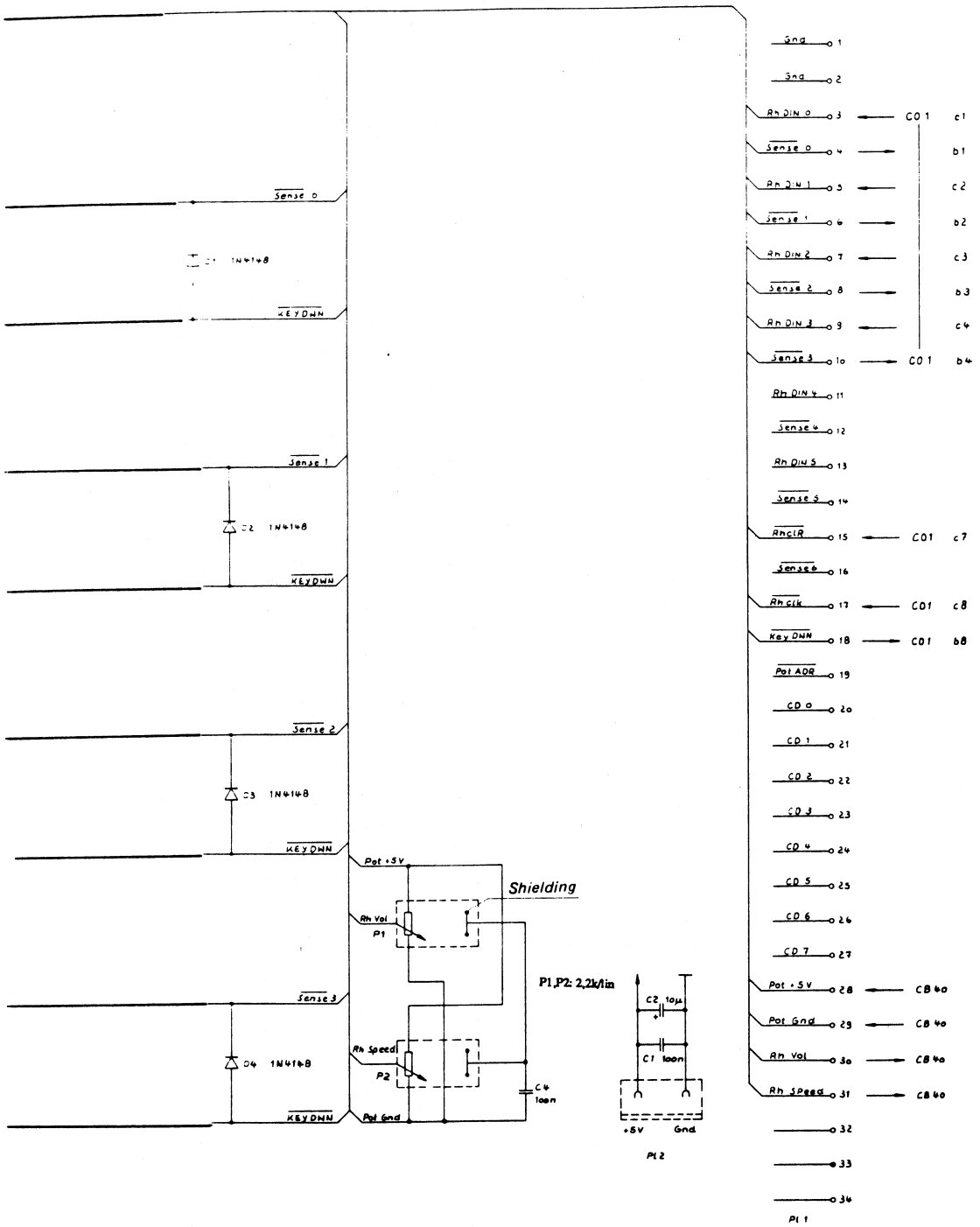
CB 49, Component layout



CB 49, Schematic diagram



CB 44, Schematic diagram


Gnd 1
Gnd 2
Rh DIN 0 3
Sense 0 4
Rh DIN 1 5
Sense 1 6
Rh DIN 2 7
Sense 2 8
Rh DIN 3 9
Sense 3 10
Rh DIN 4 11
Sense 4 12
Rh DIN 5 13
Sense 5 14
RhCLR 15
Sense 6 16
Rh Clk 17
Key DWN 18
Pot ADR 19
CD 0 20
CD 1 21
CD 2 22
CD 3 23
CD 4 24
CD 5 25
CD 6 26
CD 7 27
Pot +5V 28
Pot Gnd 29
Rh Vol 30
Rh Speed 31
32
33
34
Pl 1
CO1 c1
CO1 b1
CO1 c2
CO1 b2
CO1 c3
CO1 b3
CO1 c4
CO1 b4
CO1 c7
CO1 c8
CO1 b8
CB 40
CB 40
CB 40
CB 40
Sense 0
Sense 1
Sense 2
Sense 3
KEYDWN
D1 1N4148
D2 1N4148
D3 1N4148
D4 1N4148
Pot +5V
Rh Vol
P1
Rh Speed
P2
Pot Gnd
Shielding
P1,P2: 2,2k/lin
C4 100n
C2 10µ
C1 100n
+5V
Gnd
Pl 2

1/1113

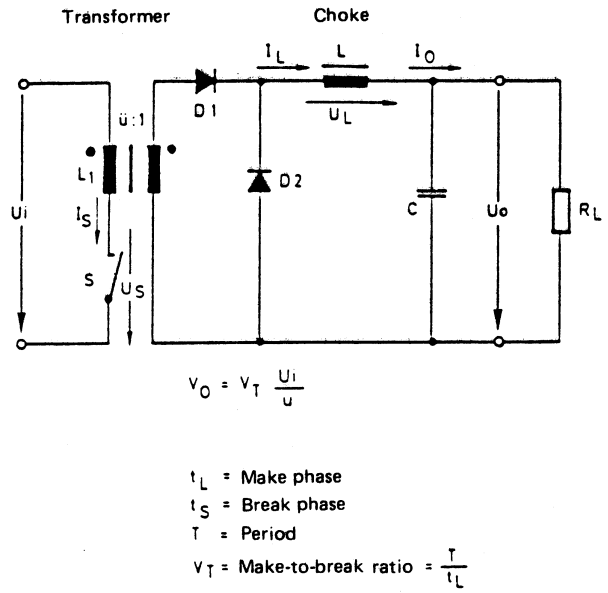


Fig. 1, Circuit diagram of a flow transducer

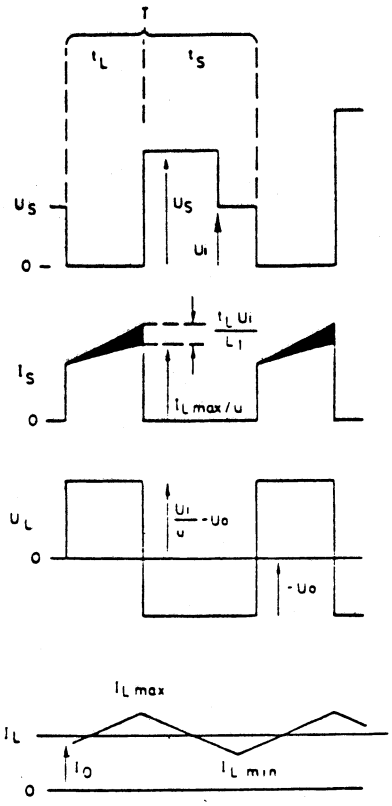


Fig. 2, Voltage and current curves of the transducer

C. Peripherals

1. PS21 (Switching Power Supply)

The switching power supply PS 21 operates on the flow transducer principle. This transducer principle makes it possible to generate several output voltages with high efficiency; the ripple of the output voltages is low. Fig. 1 shows the circuit diagram of such a transducer; Fig. 2 shows the respective (idealized) voltage and current curves.

During the make phase tL (S closed), the diode D 1 also conducts current; energy is transferred to the load circuit RL (hence the name flow transducer). Simultaneously, choke coil L receives energy with the linearly increasing current IL. Diode D 2 is not conducting.

If switch **S** is open, D 1 is polarized in the blocking direction and therefore de-energized. Because of the energy stored in choke coil L, the current proceeds through L and hence through the load circuit in the same direction, the now-conducting diode D 2 acting as a freewheeling diode. Since UQUT is approximately constant, the choke current again decreases linearly. C filters the starting voltage UOUT. The magnetic energy forcibly absorbed from the transformer during the make phase - represented by the hatched magnetization current component of the switching circuit Is - is undesired for the operation of the circuit. It must be absorbed by suitable means, transmitted back to DC source U or otherwise utilized. Thus, the voltage at the transformer or the switch (U_s) is at the same time restricted.

Let us consider the actual circuit of the power supply PS 21. The major components of the circuit are easily identified:

The transformer HFT 2 with the primary winding n1 and the secondary windings n2, n3, n4. The windings of choke coil PWR 1 are wound on the same core. This principle permits relatively good regulation of the +/-15 V outputs. The +5 V output is filtered by choke coil PWRI 2. D5. . D 8 are extremely rapid rectifier diodes and DD 1 is a high-current Schottky dual diode. C 9, 10, 11 are electrolytic capacitors with excellent high-frequency (HF) properties. The role of the switch is played by a power FET, 0 1. The network R 47, C 14, ZD 3, D 10 is selected so that the magnetizing energy is reliably absorbed and the voltage at the drain limited to about 90 V

There are various possibilities of keeping the output voltage of a switching power supply on a constant level. We chose a technique called "constant frequency, variable make-to-break ratio".

In the PS 21 we are working with the UC 3842, a very modern integrated circuit. In the overall circuit diagram, the internal structure of the IC is indicated schematically. We can best understand the function if we "run through" a working cycle.

The oscillator runs at a frequency of about 100 kHz. The positive wave shape sets the flip-flop and hence the DRIVE output; Q 1 switches on (make phase). The current I_s now flows in the primary winding, Q 1 and R 18 (Fig. 2). The voltage developed across R 18 (which is proportional to the current I_s) is applied to the positive input of the comparator. (The filter R 34, C 28, R 45, R 33, C 27 and R 44 keeps out interfering high-frequency oscillations). Once this linearly increasing voltage has reached the level at the negative input, the comparator switches, resetting the flip-flop; the drive output goes to 0, Q 1 opens and we are now in the break phase.

The cycle starts over again with the next positive edge of the oscillator. Let us again consider that the current Is (and hence the voltage at the positive input) rises as a linear function of time and let us change the voltage at the negative input.

If we make this voltage more positive, it will take longer for the linearly increasing voltage to be reached at the other input; the make phase is longer. Accordingly, the make phase becomes shorter if we reduce the voltage. The length of the make phase and hence the make-to-break ratio therefore depends on the voltage at the negative input.

This voltage is provided by the (inverting) control amplifier, which is also integrated. Its positive input is connected to the internal +2.5 V reference voltage; its negative input is connected via the voltage divider R 42, R 43 to the 5 V output of the power supply. If the voltage at the output decreases (because of the increased load), the amplifier output, that is, the comparator threshold, becomes more positive and the make phase becomes longer. Thus the output voltage rises again to 5 V and the control process is concluded. The entire system also naturally functions in the other direction.

The network R 30, C 24, D 11 generates a positive "ramp" during the make phase. Via R 31, this ramp is added to the "current ramp" and thus guarantees stable
no-load operation, however, it also limits the maximum make-to-break ratio (via comparator IC 3a and Q 3) to approximate 0.6.

Another feature of the control IC must be mentioned. It exhibits Schmidt trigger behavior relative to its supply voltage (pin 7). These thresholds are about 16 V and 10 V. This means that over 16 V, it begins functioning and below 10 V it "switches itself off."

In Practical Terms This Means That:

After the AC voltage is switched on, we have about +50 V at the charging electrolytic capacitor C 13. At electrolytic capacitor C 20, the voltage rises relatively slowly (R 17 = 10k); the IC draws a current of about 1 mA. When the 16 V threshold is reached, the IC and hence the power supply, starts. The output voltages build up, and a +15 V output then starts to supply the IC via R 9 and D 9 (the IC's consumption is now 6.8 mA). If this takeover does not occur for some reason, the elevated consumption at R 17 causes an increased voltage drop, so the voltage at C 20 drops rapidly below 10 V; the IC switches off again, the consumption drops to 1 mA, and the process repeats itself cyclically.

The comparators IC 3b, c, d are responsible for current limitation on the secondary side. The output currents are sensed via R 13, R 14, R 15. The respective comparators are correspondingly biased. When the threshold is reached (5V about 10A, +1-iSV about 1.5 A), the comparators switch (NPN open collector outputs) and bring about a lower make-to-break ratio via Q 3; the corresponding output becomes the constant voltage source.

If the load increases (to a short circuit), the output voltages decrease. At 10 V at the 1 5 V output, the control IC switches off and the power source goes into the above-described cyclic "start test" mode. C 25, D 12, R 39 provide a "soft start".

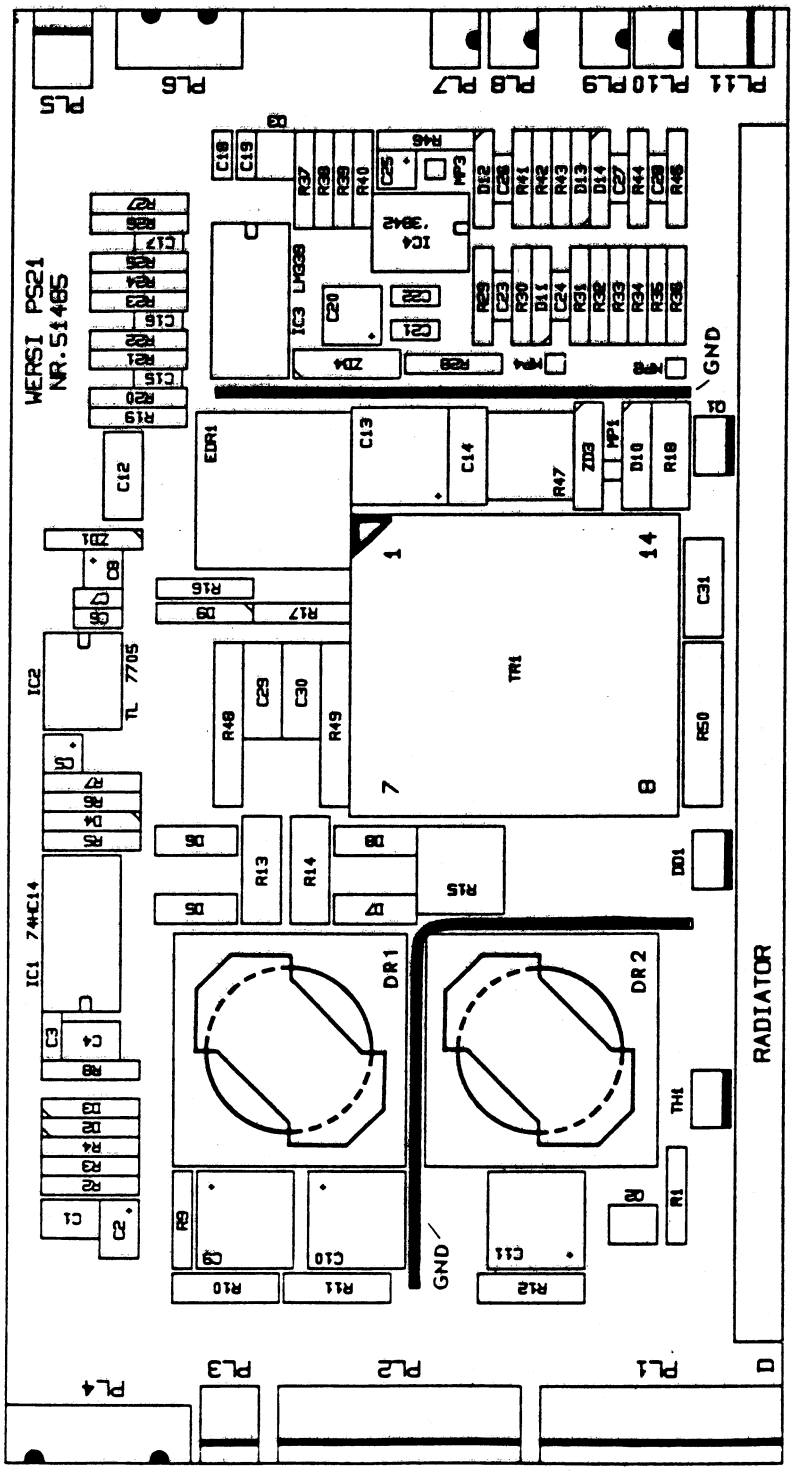
Th 1 and Q 2 form the "crowbar" circuit, which protects the 5 V output from over-voltage by producing a short circuit at about 5.5 V.

IC 2 is supplied by R 16 and generates the system reset.

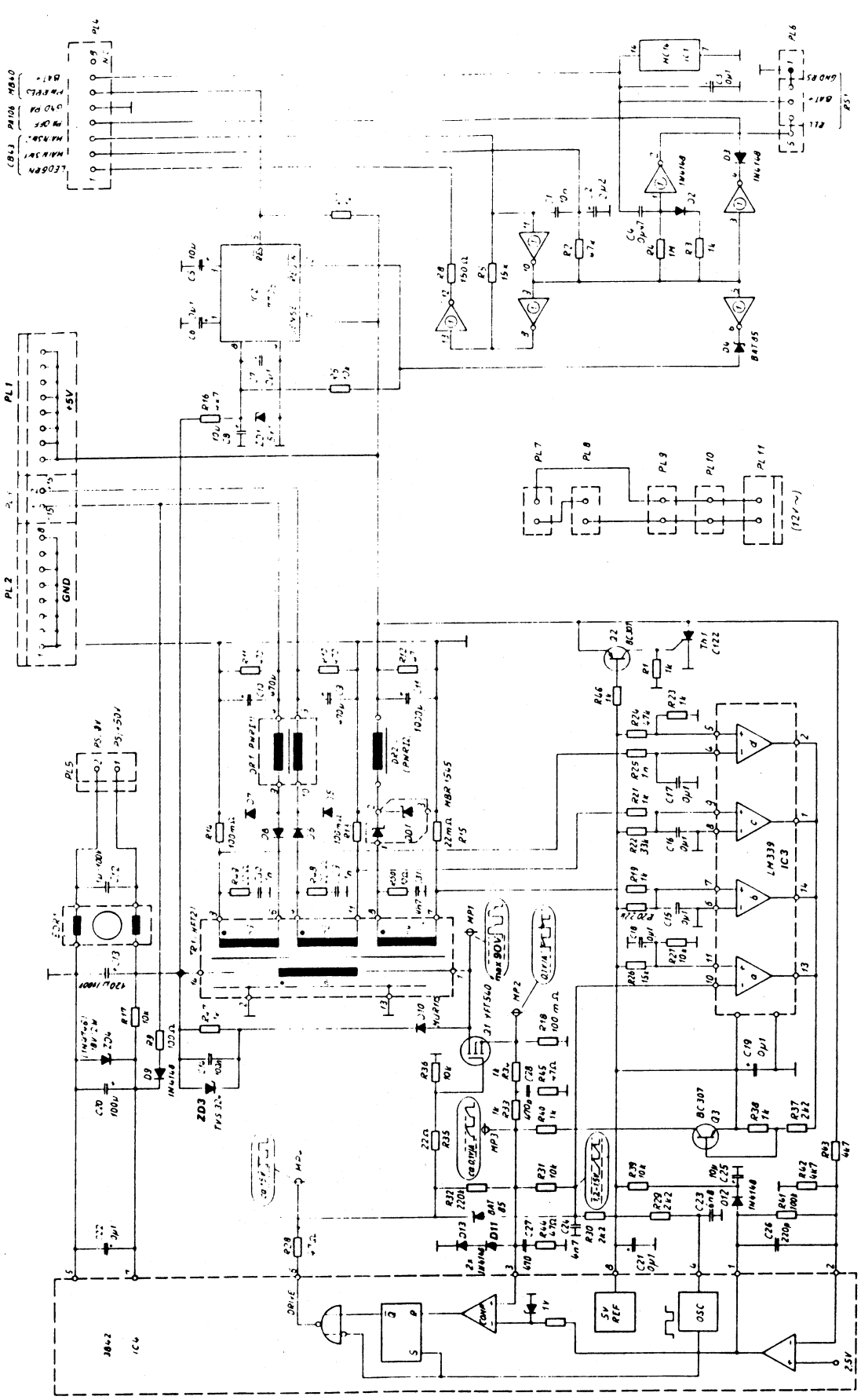
IC 1 is not exactly a part of the power supply unit. It is supplied from the outside (BATT) and acts - in combination with the on/off switch on the control panel CB 43 and the relay on RS 1 - like an electronic switch.

Technical Data PS 21:

Design:	Single-ended flow transducer		
Operating frequency:	about 100 kHz		
Input:	50 to 55V		
Output:	+5 V (+/-2%)	max.	10 A
	+15 V (+1-10%)	max.	1.5 A
	-15V (+5/-10%)	max.	1.5 A



PS 21, Component layout



PS 21, Schematic diagram

2. CB 45 (Main Connection Board)

The connection board CB 45 carries the MIDI and the RS 232 interfaces, apart from the audio outputs headphones, Main LIR and tape.

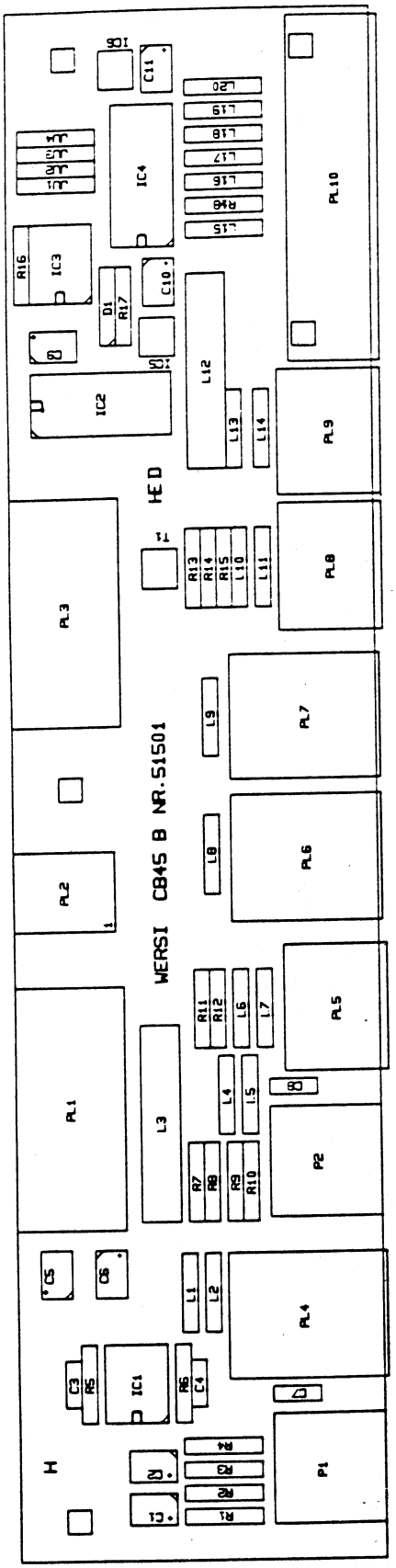
With regard to the MIDIIRS 232 interface, let us mention that in "receive mode" the circuit switches over from MIDI to RS 232 (with multiplexer IC 2, HC 157) only if DSR (pin 6 at the Sub-D-socket) is at about +10 V. This signal has to be sent by the connected computer. Also the CTS signal has to be generated by the computer (if not, set this pin at +12 V).

The board sends MIDI OUT and RS 232 simultaneously.

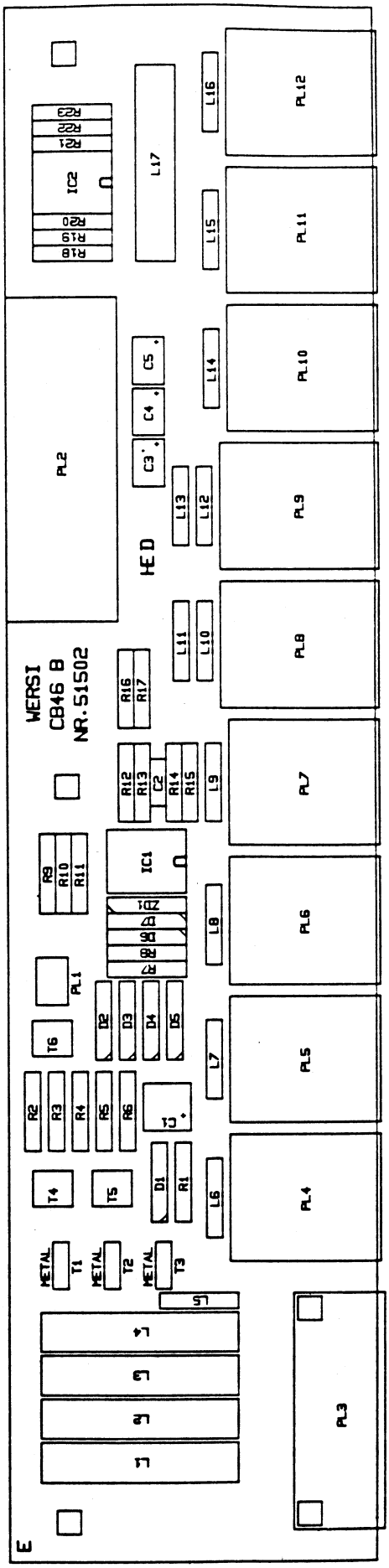
3. CB 46 (Additional Connection Board)

On this board there are some additional audio outputs and a Leslie control circuit. This circuit recognizes whether a Leslie is hooked up via the 15-pin Sub-D-socket and sends this information to the master via LESINS. The master switches the instruments routed via WV to the Leslie amplifier, which transmits the amplified signal to the Leslie.

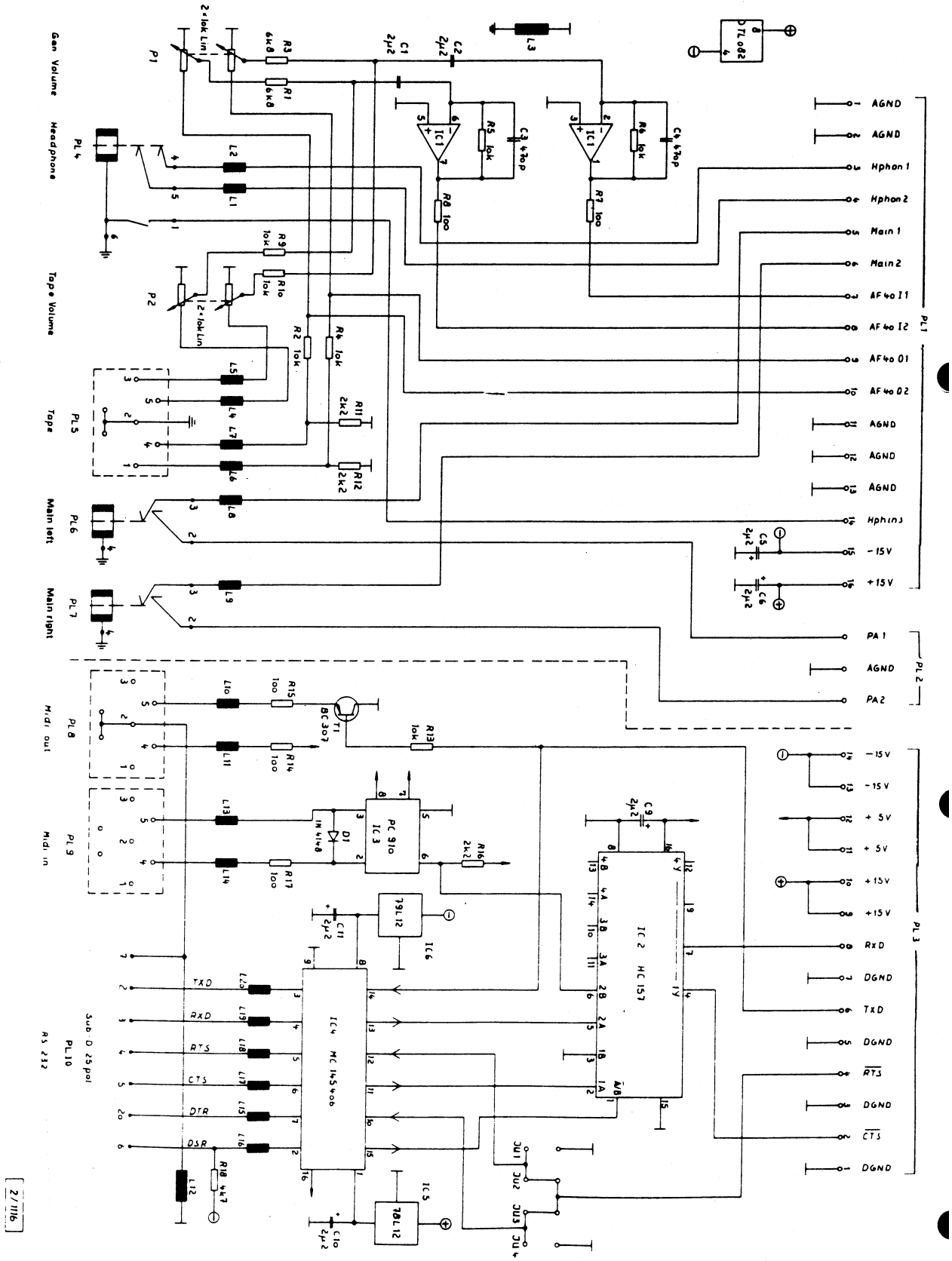
The rate can be set with SLOW and FAST. These open collector outputs can, for instance, control the relays (the necessary voltage - 12 V - is also applied to Sub-D), which effect the slow/fast switchover of the Leslie.



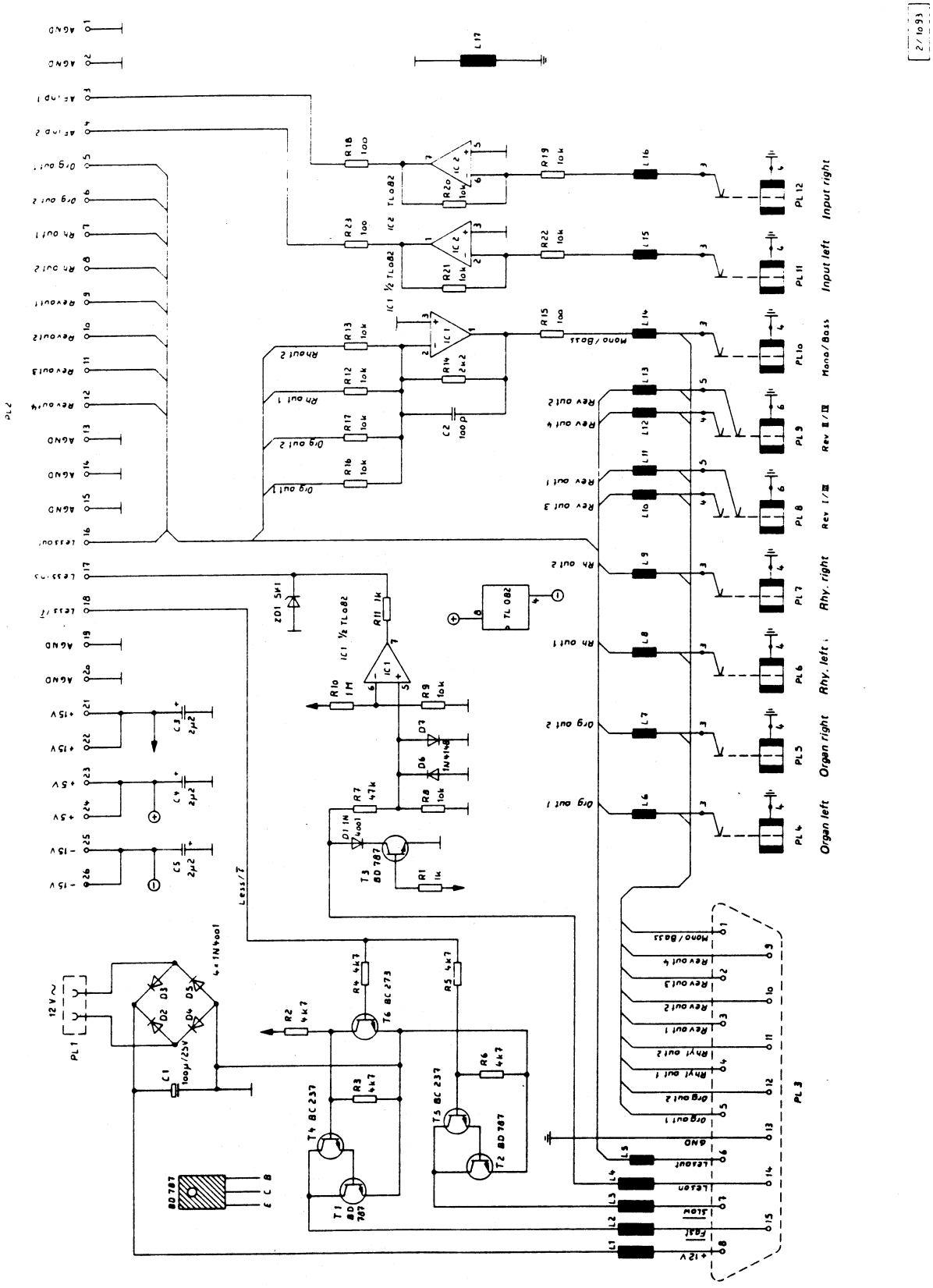
CB 45, Component layout



CB 46, Component layout



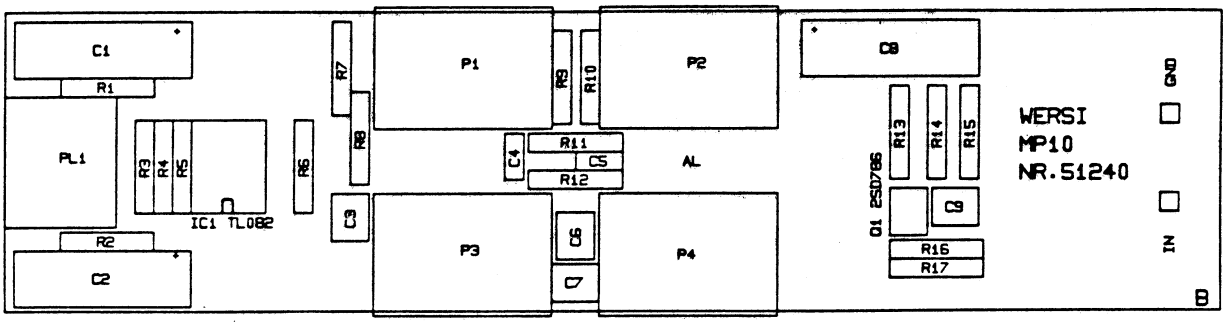
CB 45, Schematic diagram



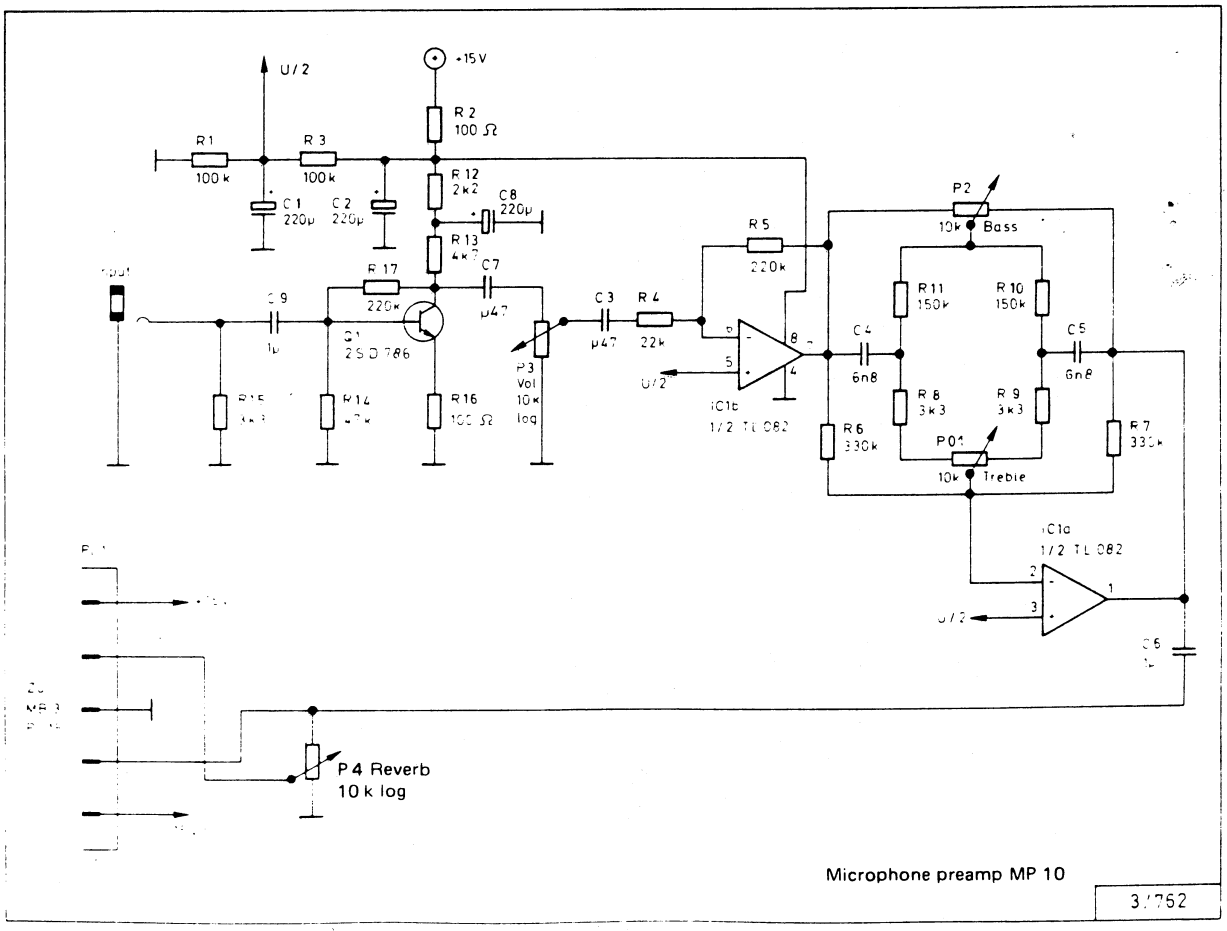
CB 46, Schematic diagram

4. MP 10 (Microphone Amplifier)

This board carries- the microphone amplifier and the tone control. The portion to be reverberated can be adjusted with the reverb potentiometer



MP 10, Component layout



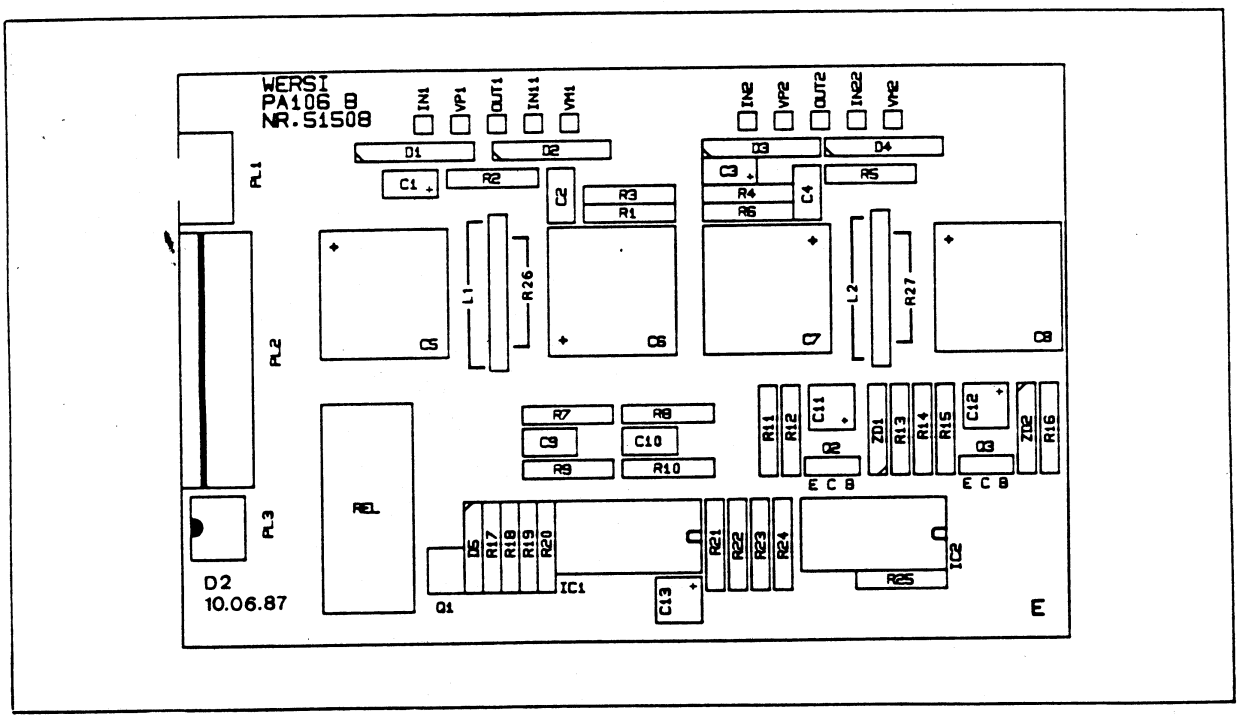
MP 10, Schematic diagram

5. PA 106 (Power Amplifier)

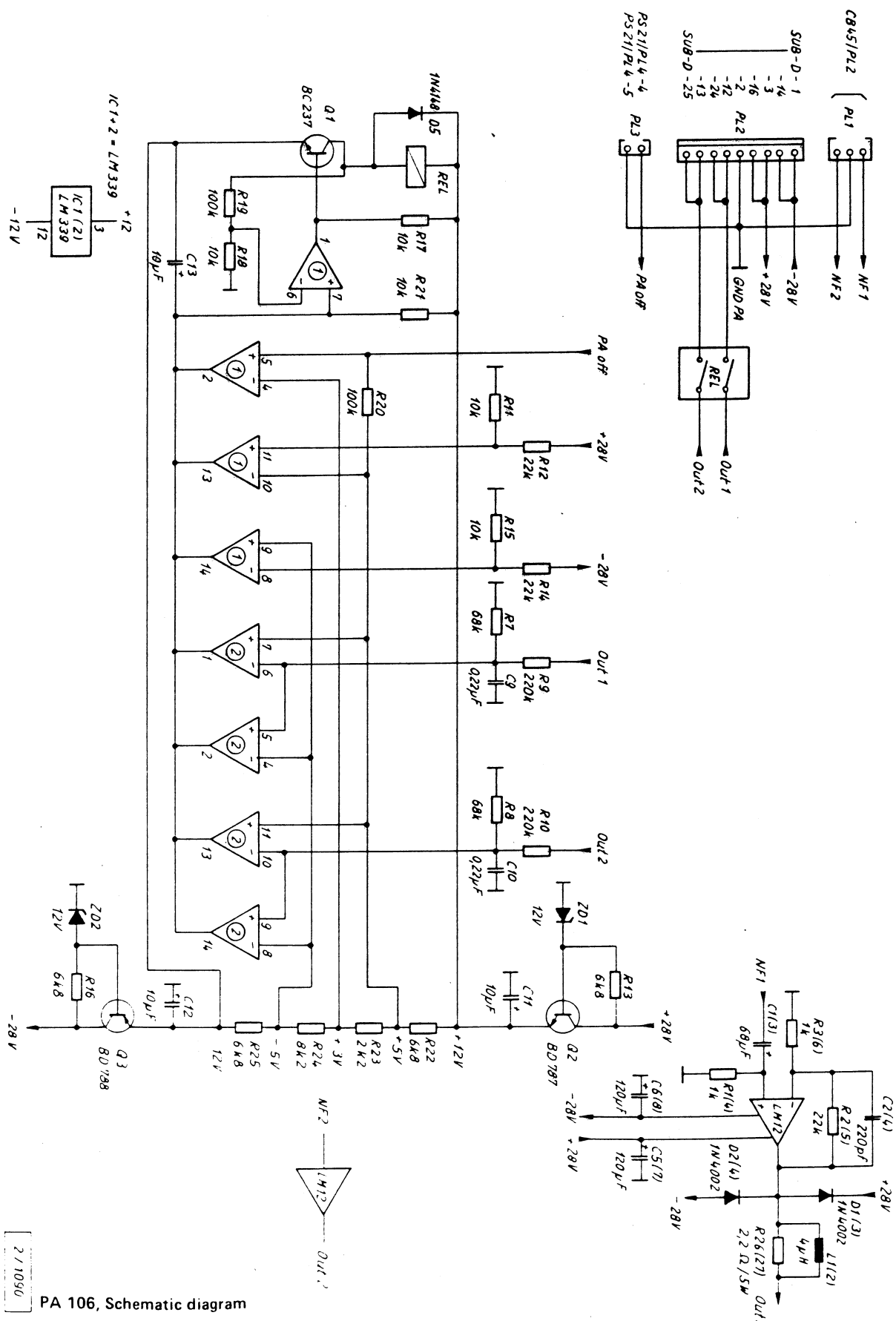
This board carries, apart from the actual stereo amplifier (2 xLM 12), a relatively extensive protective circuit. This circuit connects the outputs of the amplifier to the loudspeakers only if the following pre-conditions are given:

1. the supply voltages of the amplifier are present;
2. no DC voltage is at the amplifier outputs;
3. the switch-on circuit of the power supply opens the amplifier output (PAOF F).

The switching on will be delayed C 13, R 21 to avoid amplification of "start-up" noise and power surges generated by the organ.



PA 106, Component layout



2 / 1090

PA 106, Schematic diagram

6. PU 1 (Power Chassis, Plug-In Board)

This board can be found together with the transformer and the PC Board RS 1 in the Power Chassis NE 60.

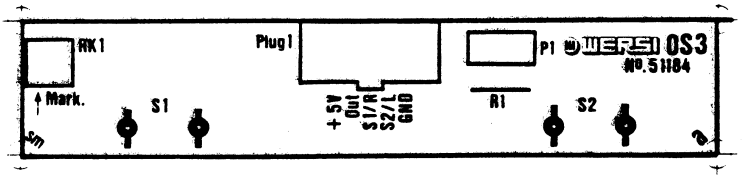
Apart from the fuses, this board carries the electrolytic capacitors for filtering the supply voltages (power supply and amplifier). Furthermore, this board acts as connection board for the swell pedal (05 3), loudspeaker and relay board (RS 1).

7. RS 1 (Relay Board)

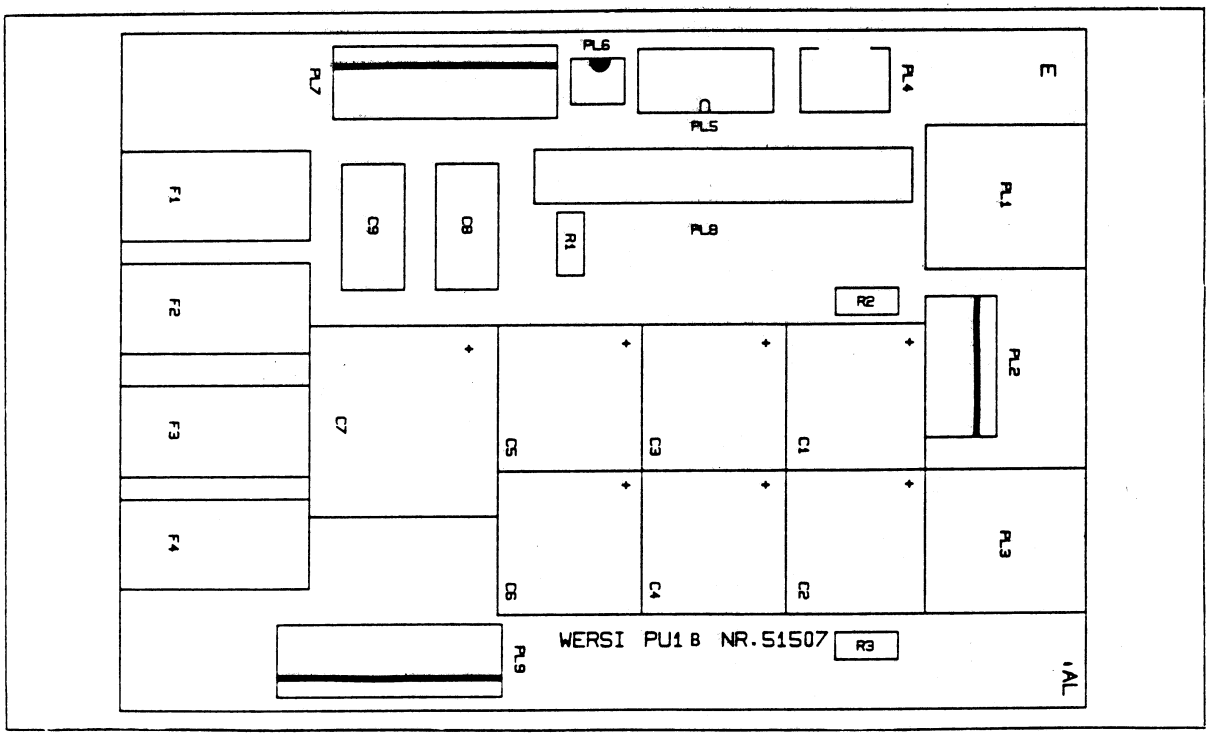
In the "stand-by" mode (green LED in on/off switch is illuminated) this board supplies the organ with the BATT voltage and switches - via the AC line relay -the entire organ on or off when the on/off switch is depressed.

8. OS 3 (Swell Pedal, Footswitch)

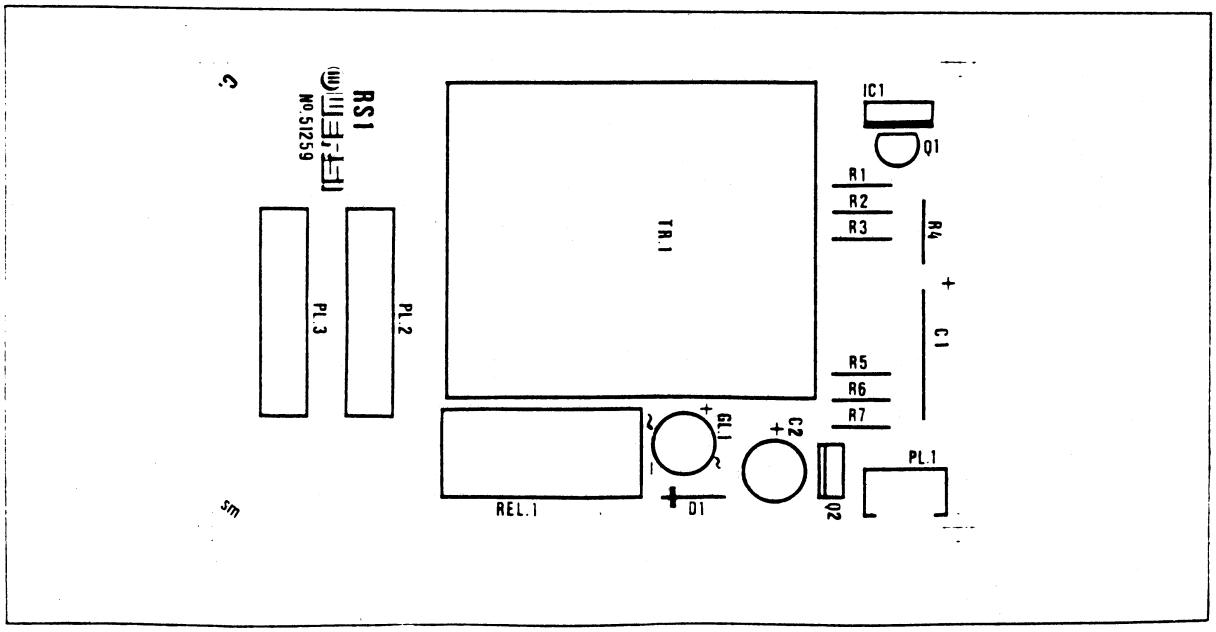
This board has two footswitch connections as well as the reflex coupler, which supplies a current of 0 (low volume) to 0.6 mA (high volume), depending on the position of the swell pedal. This range can be fixed with the potentiometer.



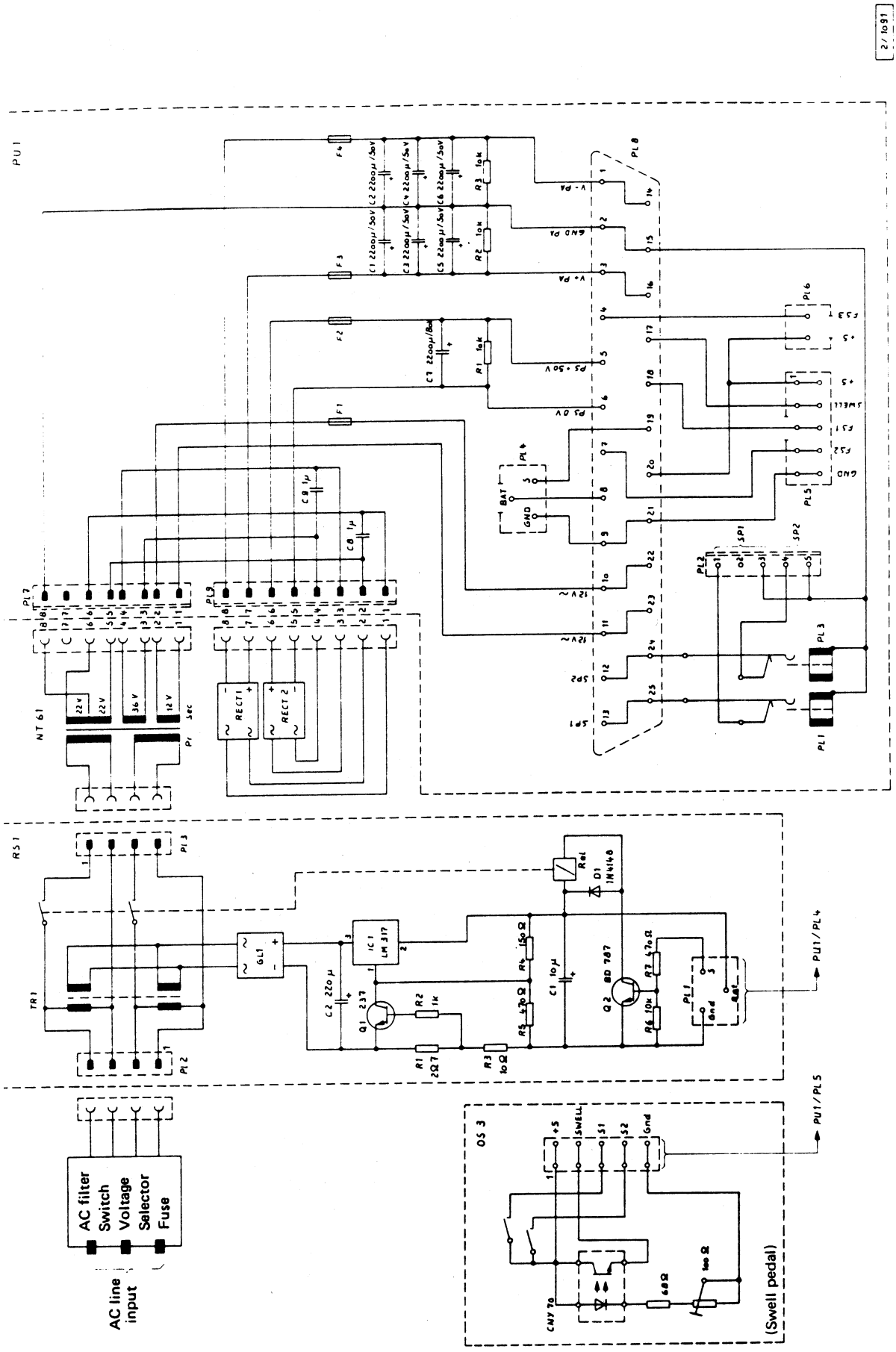
OS 3, Component layout



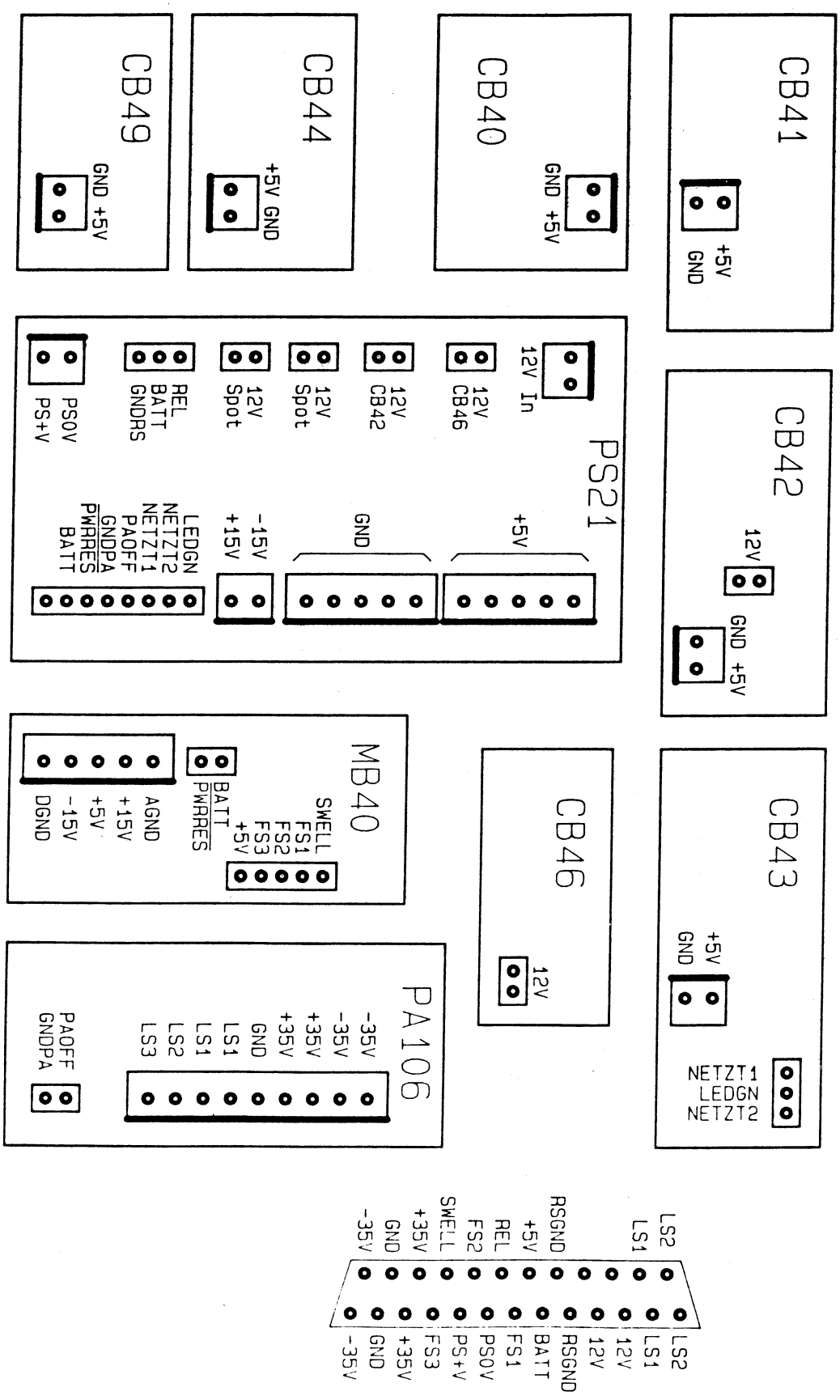
PU 1, Component layout



RS 1, Component layout

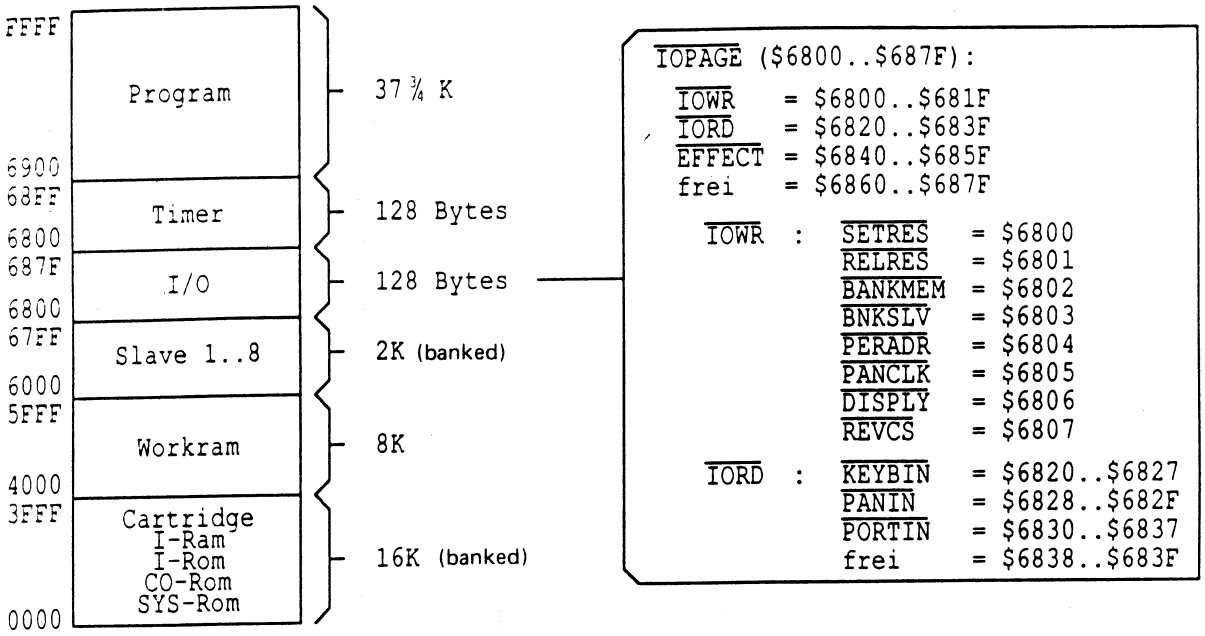


Power chassis NE 60, schematic diagram

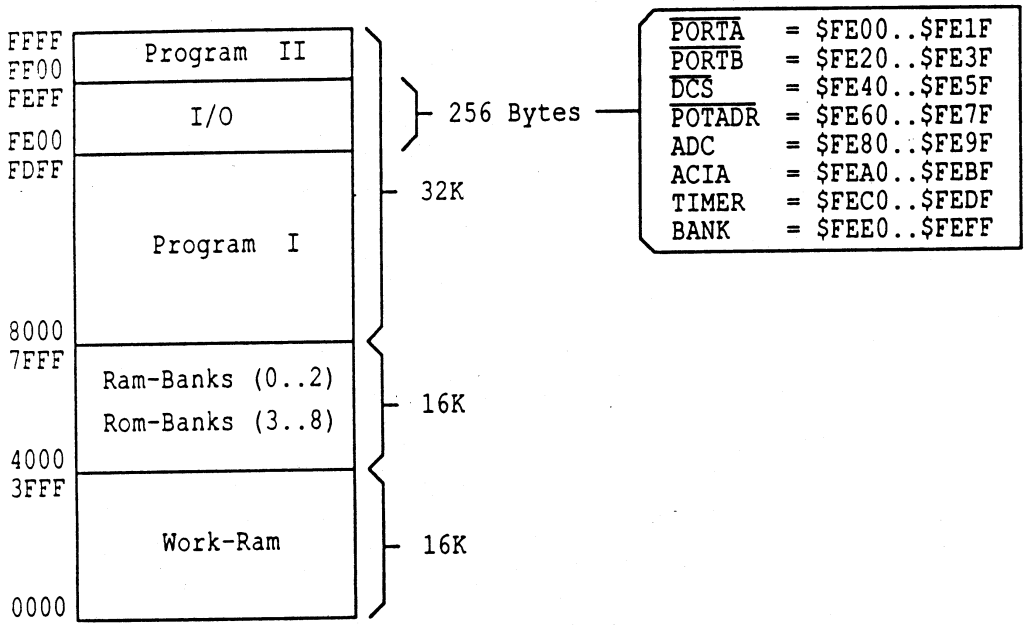


Power Connections

Memory Map NST8



Memory-Map C01 :



D. GLOSSARY OF MICROCOMPUTER TERMS

If the technical data presented in this manual is your first contact with microcomputer technology, you have doubtless encountered some concepts, which are new to you and will need some explanation. Some of the more frequently used digital "buzzwords" are presented here in alphabetical order:

Address - A unique and selectable position in a memory device (see RAM, ROM, EPROM) where data can be stored and retrieved.

Address Bus - A collective term for the lines by which address data is transferred from the central processing unit (CPU) to the memory devices.

A/D Converter - Analog- to-Digital converter; a device that converts analog data, i.e. data that is continuously variable, such as audio, into digital data for processing and storage in a digital system.

Bit - Short for "binary digit," or the smallest unit of information in the binary number system. A bit represents one of two fixed states, a "1" or a "0".

Bus - Collectively, the lines on which data is transferred; ex.: data bus, address bus, control bus.

Byte - A sequence of 8 adjacent bits, considered as a digital unit.

Chip - A small piece of semiconductor material on which integrated circuits are fabricated; the actual circuit of an IC.

Clock - The timing signals used in a microprocessor system; the circuit used to generate these signals.

CPU - Central processing unit; the unit in a computer' that performs and controls the execution of instructions, performs arithmetic functions, and generates clock signals.

D/A Converter - Digital-to-analog converter; converts digital data into analog signals such as control voltages or audio.

Display - A visual indicator used as a means to read out digital data.

EPROM -- Erasable programmable read-only memory (see ROM); a ROM capable of storing new data; existing data can be erased and new data can be read into the ROM.

Hardware - The components which make up the computer proper: the electronics, control devices, readouts, etc. The hardware carries out the computer functions in accordance with the software entered into it. See Software.

Interface - A takeoff point for connecting a computer function to an "outside world", or peripheral, device.

LED - Light-emitting diode; a semiconductor device that emits light when voltage is applied to it. Used as an indicator.

Master Processor - In a multi-processor system, the processor that is responsible for the central control and execution of instructions for the rest of the system -

Microprocessor A single-chip (IC) central processing unit.

Program A series of instructions which define the steps a computer must follow to perform a given function.

RAM - Random access memory; a memory into which data may be stored or read out in any order at random. A RAM loses its stored data if its supply voltage is removed, and therefore must be protected against memory loss by a battery supply.

ROM -Read-only memory; contains permanent data entered at manufacture. The data cannot be altered and remains even if the supply voltage is removed.

Slave Processor - In a multi-processor system, a processor which is subservient to the master proces; or, from which it receives its instructions and control.

Software -- The computer programs, procedures and documents necessary for the operation of a computer system.

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